Reduction in Capacitor of Flying-Capacitor for a 3+1-Level Converter

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Abstract— This paper presents a space-vector modulation (SVM) strategy to reduce the required flying-capacitor (FC) capacitance in a 3+1-level flying-capacitor converter (FCC). In the conventional 3+1-level modulation approach, FC charge and discharge control depends only on the phase with the highest current amplitude, leading to large FC voltage fluctuations and a need for larger FC capacitance. To solve this problem, the proposed method manages FC charging and discharging during both the maximum- and minimum-current phases. Simulation results demonstrate that the proposed approach reduces the FC voltage fluctuation rate to 1.75%, a 3.67-percentage-point reduction, and suggests a potential 72.2% decrease in the required FC capacitance under the same voltage-fluctuation criterion. Experimental results also confirm a 2.56-percentage-point reduction in FC voltage fluctuation rate while maintaining THD characteristics comparable to those of the conventional method.

Keywords— Flying capacitor, Multilevel converter, Space vector modulation (SVM)

I. INTRODUCTION

Two-level converters have been widely employed in practical applications because of their simple circuit configuration. However, they suffer from high harmonic contents in phase currents and line-to-line voltages, since the output voltage ripple caused by switching has the same amplitude as the dc-link voltage. To address this issue, multilevel converters have been proposed [1] – [2]. By connecting multiple semiconductor switches in series, multilevel converters increase the equivalent switching frequency and reduce harmonics in phase currents and line-to-line voltages while enabling the use of lower-voltage devices.

Various circuit topologies, such as flying-capacitor converters, diode-clamped converters, and T-type converters, have been proposed to generate multilevel output voltages [1] – [2]. Among them, the flying-capacitor converter (FCC) is characterized by its ability to actively control the flying-capacitor (FC) voltage through switching operations [3] – [5].

In the FCC, the FC voltage must be maintained at a constant value through charge and discharge control. Carrier phase-shifted PWM (CS-PWM) is a representative modulation method for this purpose [5] – [6]. In CS-PWM, carrier waves with evenly shifted phases are generated according to the number of voltage levels in the main circuit, and gate pulses are obtained by comparing these carriers with the three-phase voltage references. However, because CS-PWM does not explicitly optimize the selection of voltage vectors with respect to the reference vector, its ability to suppress line-to-line-voltage harmonics and phase-current ripple is limited compared with SVM.

To overcome this drawback, space vector modulation (SVM) has been proposed [6] – [10]. By applying SVM, the output voltage vector of the FCC can be controlled arbitrarily, and switching sequences can be designed according to the designer's intention. For example, phase-current ripple can be reduced while maintaining the desired output voltage. However, because the FCC does not possess a natural voltage-balancing mechanism, additional control is required to maintain the FC voltage at half of the input voltage.

As an extension of the conventional three-level converter, a 3+1-level converter has been proposed [11]. In SVM, the timing of FC charge and discharge in each phase can be intentionally maintained in an unbalanced state. By using this feature, one additional output voltage level can be generated, bringing the total to four. This modulation method is referred to as 3+1-level SVM [11]. Since 3+1-level SVM can generate a four-level output voltage while retaining the conventional three-level circuit configuration, harmonics in the line-to-line voltage and phase current can be further reduced.

However, in the 3+1-level SVM proposed in [11], charging/discharging control for the FC voltage is performed only once per cycle at twice the voltage-reference frequency, resulting in large FC voltage fluctuations. Consequently, large-capacitance flying capacitors are required to suppress FC voltage fluctuations in the conventional 3+1-level SVM. The use of such large capacitors, however, hinders further miniaturization of the overall converter.

To address this issue, this paper proposes a new SVM scheme for a 3+1-level FCC to suppress FC voltage fluctuation and reduce the required FC capacitance. Unlike the conventional 3+1-level SVM, which determines FC charge/discharge control only from the maximum-current phase, the proposed method additionally utilizes the minimum-current phase during vector selection. This increases the opportunity to compensate for FC charge imbalance within a voltage-reference cycle, thereby reducing FC voltage ripple without modifying the converter hardware.

II. FLYING CAPACITOR CONVERTER

Fig. 1 shows the circuit diagram of a three-phase, three-level FCC. The three-level FCC consists of four semiconductor switches connected in series to form a leg, and three such legs connected to form a three-phase configuration. Within each leg, the upper two switches form the upper arm, and the bottom two switches form the lower arm. In this paper, the switching state of the n-th phase is represented by (S_{n1}, S_{n2}),

where S_{n1} and S_{n2} denote the ON/OFF states of the two switches in the upper arm. Here, S_{n1}, S_{n2} = 0 and 1 denote the OFF and ON states, respectively. Thus, the switching state of one leg can take one of the four switching patterns listed in Table I.

The four switching patterns of each leg are collectively referred to as the "state." Each state is represented by a single-digit code indicating the switching configuration of a leg. As summarized in Table I, states 0 and 3 bypass the FC, whereas states 1 and 2 insert the FC into the current path.

Accordingly, the phase voltage is 0 in state 0, v_{fc} in state 1, V_{dc} - v_{fc} in state 2, and V_{dc} in state 3. Since the FC is involved only in states 1 and 2, FC charging and discharging can occur only in these states. Thus, balancing the FC voltage requires appropriate charge/discharge control in each phase.

Whether the FC is charged or discharged is determined by the phase current direction. As shown in Table I, when the phase current is positive, state 1 discharges the FC and state 2 charges it. In contrast, when the phase current is negative, state 1 charges the FC and state 2 discharges it. Therefore, FC voltage balancing requires appropriate selection of the state according to both the desired output voltage and the phase current direction.

From the above discussion, the FC charging or discharging operation of the FCC is determined by the switching state and the phase current direction. Given this characteristic, a modulation scheme capable of generating the desired voltage vector while properly controlling the FC voltage is indispensable. The next section explains SVM, which is a representative control method.

III. Three-Level Space Vector Modulation (SVM)

In the three-level FCC SVM method, the FC voltage is typically balanced at one half of the input voltage. The corresponding voltage vector diagram is shown in Fig. 2. Voltage vectors corresponding to different switching states may occupy the same position on the coordinate plane; these are referred to as redundant vectors. Excluding redundant vectors, 19 basic voltage vectors are available for selection. The choice among redundant vectors depends on the FC voltage. For example, when the FC is over-discharged, the vector that charges the corresponding phase is selected.

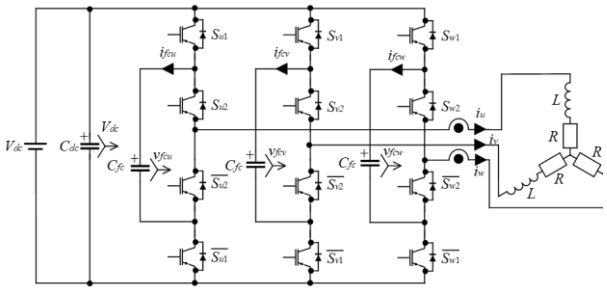

Fig.1. three-phase-three-level FCC.

TABLE I. The relation between the switching function and the charging/discharging state of FC (* = U, V, W).

Switching (S_{*1}, S_{*2})		0, 0	0, 1	1, 0	1, 1
state		0	1	2	3
Output Voltage		0	v_{fc}	V_{dc} - v_{fc}	V_{dc}
FC Charging/ Discharging	$i_* > 0$	Neutral	Discharging	Charging	Neutral
	$i_* < 0$		Charging	Discharging	

Based on these basic vectors, the desired voltage vector is synthesized by selecting three vectors. To reduce current ripple, it is desirable to choose vectors located close to the reference vector. Therefore, appropriate basic-vector selection is essential for achieving the desired output voltage while suppressing current ripple.

This section describes the basic vector selection method when the FC voltage is balanced at one half of the input voltage. The next section introduces the conventional 3+1-level SVM method [11], in which an intentionally unbalanced FC voltage is utilized to further reduce line-to-line-voltage and phase-current harmonics.

IV. Conventional 3+1-Level SVM [11]

Fig. 3 shows the voltage vector diagram of the conventional 3+1-level SVM when the FC voltage is intentionally maintained at 40% of the input voltage. Owing to this intentional imbalance, basic vectors that are redundant in the three-level case are separated from one another. As a result, the number of distinct selectable basic vectors increases from 19 in Fig. 2 to 49 in Fig. 3.

This increase in the number of selectable basic vectors improves the flexibility of vector selection. Compared with the three-level case, the denser vector distribution in Fig. 3 makes it possible to select a basic vector closer to the desired output voltage vector, which is expected to reduce phase-current ripple. However, in the 3+1-level FCC, vector selection must also take into account the FC charging and discharging states of each phase.

In the conventional 3+1-level SVM, FC-voltage control is determined mainly by the phase with the maximum current. Because the maximum-current phase carries the largest current flowing into and out of the FC, it has the greatest influence on the FC voltage. Therefore, the conventional method focuses on the charging and discharging behavior of

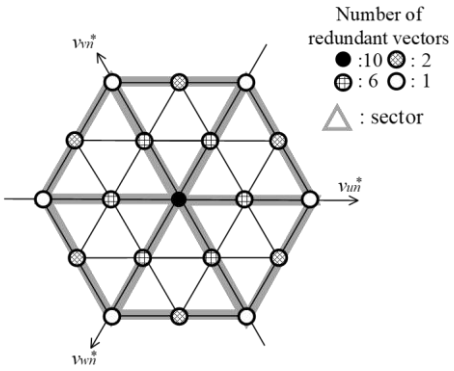

Fig. 2. Output voltage vector on space vector modulation.

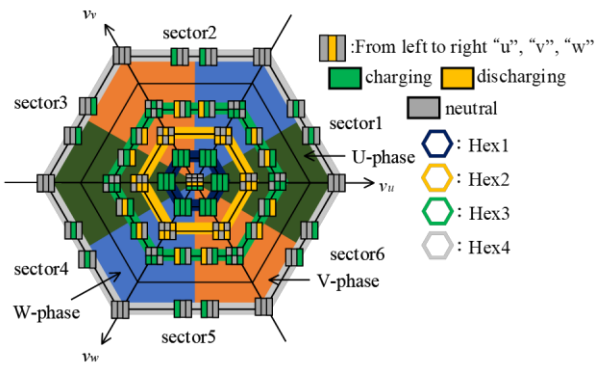

Fig. 3. Voltage vector diagram with FC charging and discharging.

the FC in the maximum-current phase in order to maintain the intended unbalanced FC voltage.

Fig. 3 classifies the selectable basic vectors according to their charging/discharging effect on the FC of the maximum-current phase. In this figure, Hex1 and Hex3 denote the vector groups that charge the FC, Hex2 denotes the vector group that discharges the FC, and Hex4 denotes the vector group that maintains the FC charge/discharge state. The color of each vector indicates which phase is the maximum-current phase: green, orange, and blue correspond to the u-, v-, and w-phases, respectively, assuming unity power factor.

Figs. 4 and 5 illustrate how the conventional method selects vectors to regulate the FC voltage of the maximum-current phase. In the example of Fig. 4, the basic vector indicated by the red circle is selected for the output voltage vector shown by the white arrow. If such vectors are continuously selected, the FC voltage of the u-phase, which is the maximum-current phase in this region, increases. Therefore, when the FC of the maximum-current phase must be discharged to maintain the intended unbalanced voltage, a vector belonging to Hex2 is selected, as shown in Fig. 5.

Although the conventional method can maintain an intentionally unbalanced FC voltage, its charge/discharge control opportunity is limited. In this method, the FC of the maximum-current phase is charged or discharged only once every two cycles of the voltage reference. Consequently, significant FC-voltage fluctuation remains, and a new vector-selection method is required to suppress it further. The next section presents the proposed method.

V. Proposed 3+1-Level SVM Considering The Minimum-Current Phase

In the conventional 3+1-level SVM described in the previous section, FC voltage control is determined based on the maximum-current phase. As a result, although the FC voltage of the maximum-current phase can be controlled, the FC-voltage deviation of the minimum-current phase cannot be sufficiently compensated within the same cycle, resulting in large FC-voltage fluctuations. To address this issue, this section proposes a vector-selection method that compensates the FC-voltage deviation of the minimum-current phase while preserving the conventional control of the maximum-current phase.

In this paper, a pair vector denotes a pair of corresponding basic vectors in Hex4 that preserves the conventional FC charge/discharge condition for the maximum-current phase while changing only the charge/discharge effect on the minimum-current phase. The basic idea of the proposed method is to replace the Hex4 vector selected by the conventional method with its paired vector only when the selected vector further increases the FC-voltage deviation of the minimum-current phase. In this way, the FC-voltage deviation of the minimum-current phase can be compensated without affecting the conventional control.

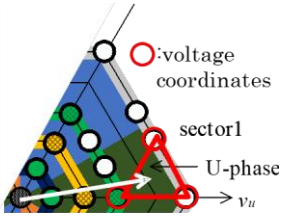

Fig. 4. Selection of voltage coordinates with FC over-discharge (max phase).

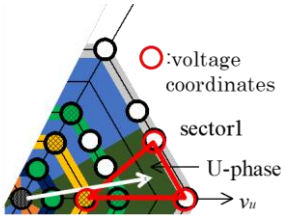

Fig. 5. Selection of voltage coordinates with FC over-charge (max phase).

First, a vector satisfying the FC charge/discharge condition of the maximum-current phase is selected according to the conventional method. Next, the minimum-current phase is identified from the three-phase currents. Then, based on the FC-voltage deviation of the minimum-current phase, the current direction of that phase, and the switching state of that phase in the selected vector, it is determined whether the selected vector acts to charge or discharge the FC of the minimum-current phase. If the selected vector further increases the FC-voltage deviation of the minimum-current phase, it is replaced with the corresponding paired vector.

This replacement is possible because, in the conventional method, two of the three selected basic vectors are located on Hex4. Therefore, by appropriately reselecting the vectors on

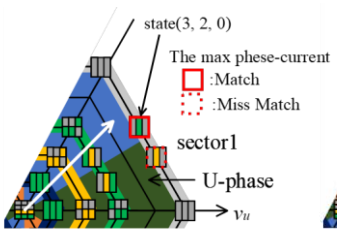

Fig. 6. During v-phase FC charging.

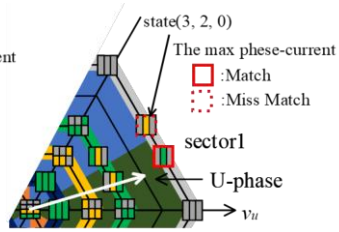

Fig. 7. During v-phase FC discharging.

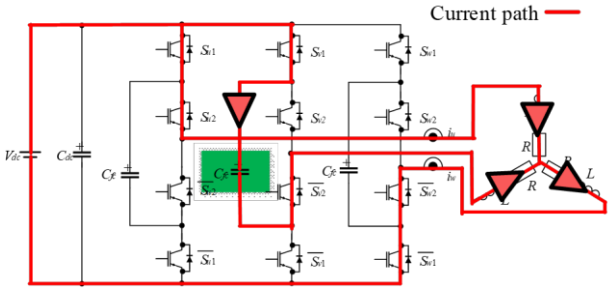

Fig. 8. Current Path When the Maximum-Current Phase Matches the Output-Vector Phase.

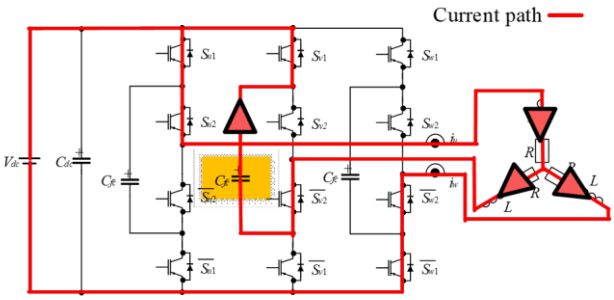

Fig. 9. Current Path When the Maximum-Current Phase Does Not Match the Output-Vector Phase.

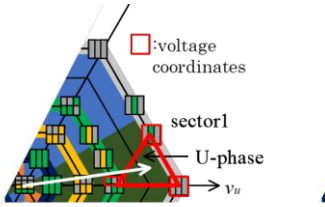

Fig. 10. Selection of Voltage Coordinates for an Over-Discharged FC in the Minimum-Current Phase.

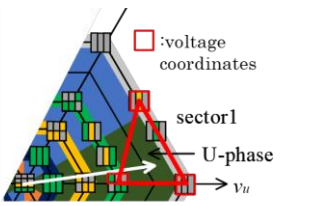

Fig. 11. Selection of Voltage Coordinates for an Over-Charged FC in the Minimum-Current Phase

Hex4, the FC-voltage deviation of the minimum-current phase can be compensated while preserving the conventional control of the maximum-current phase. Fig. 3 shows the basic vector group used for this purpose.

Whether the FC of the minimum-current phase is charged or discharged depends on the switching state of the minimum-current phase and the direction of the phase current. Under the unity-power-factor condition considered here, the maximum-current phase can be determined from the phase region of the output voltage vector. Therefore, even for the same vector on Hex4, the effect on the FC of the minimum-current phase differs depending on the phase region in which the output voltage vector is located.

As a representative example of how the charge/discharge direction depends on the output-voltage-vector region, consider the switching state (3, 2, 0). This state is shown in the voltage-vector diagrams of Figs. 6 and 7. Fig. 6 illustrates the case where the maximum-current phase determined by the output-voltage-vector region matches that associated with state (3, 2, 0), whereas Fig. 7 illustrates the case where they do not match. The corresponding current paths are shown in Figs. 8 and 9, respectively. In these cases, the v-phase is the minimum-current phase and is in state 2. In the former case, the FC of the v-phase is charged, whereas in the latter case it is discharged. Thus, the charge/discharge direction of the FC in the minimum-current phase depends not only on the switching state but also on the phase region of the output voltage vector.

From the above discussion, the vector-selection rule of the proposed method can be summarized as follows. When the FC voltage of the minimum-current phase is lower than its reference value, the paired vector that acts to charge the FC of the minimum-current phase is selected. Conversely, when the FC voltage of the minimum-current phase is higher than its reference value, the paired vector that acts to discharge the FC of the minimum-current phase is selected. In both cases, priority is given to the candidate vector that is as close as possible to the desired output voltage vector in order to suppress phase-current ripple. Thus, the Hex4 vector selected by the conventional method is replaced with the corresponding paired vector only when it further increases the FC-voltage deviation of the minimum-current phase.

Figs. 10 and 11 show representative examples of vector selection when the FC of the minimum-current phase is over-discharged and over-charged, respectively. In Fig. 10, a vector that charges the FC of the minimum-current phase is selected. In Fig. 11, a vector that discharges the FC of the minimum-current phase is selected. The overall selection procedure is summarized in the flowchart shown in Fig. 12.

By this method, the conventional FC charge/discharge control for the maximum-current phase is maintained, while the FC-voltage deviation of the minimum-current phase is also compensated. As a result, the degree of freedom for FC-voltage compensation within one cycle is increased, and FC-voltage fluctuations can be more effectively suppressed. The next section verifies the effectiveness of the proposed method through simulation.

VI. Simulation Results

To verify the effectiveness of the proposed method, simulations were conducted. The simulation conditions are listed in Table II. Fig. 13 shows the simulation results. The

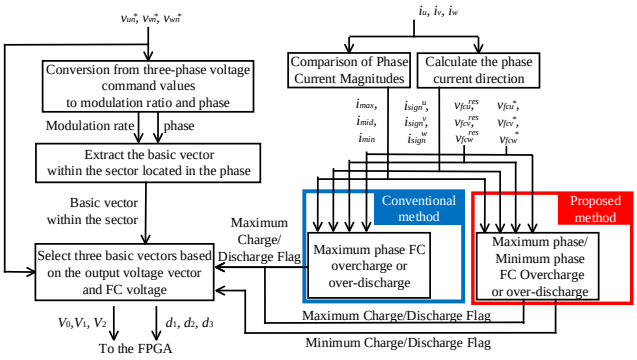

Fig. 12. Flowchart.

first half of the figure shows the results of the conventional method, and the second half shows those of the proposed method. In the proposed method, FC-voltage fluctuation is significantly reduced, and the FC voltage is maintained at 40% of the input voltage. Here, the FC-voltage fluctuation rate is defined as the peak-to-peak FC-voltage fluctuation normalized by the reference FC voltage. Table III summarizes the simulated FC-voltage fluctuation. The fluctuation rate of the proposed method is 3.67 percentage points lower than that of the conventional method, confirming the effectiveness of the proposed method in suppressing FC-voltage fluctuation.

Next, the FC capacitance required to satisfy the same voltage-fluctuation criterion as that of the conventional method was evaluated by simulation. As a result, the required FC capacitance was found to be 500 μF. Fig. 14 shows the corresponding simulation results. This corresponds to a 72.2% reduction compared with the original FC capacitance of 1.8 mF.

These results indicate that the proposed method effectively suppresses FC-voltage fluctuation and has the potential to reduce the required capacitance. The next section presents experimental results to confirm the suppression effect in hardware and to evaluate its influence on output waveform quality.

VII. Experimental Results

In the previous section, simulation results confirmed the effectiveness of the proposed method in suppressing FC-voltage fluctuation. This section presents the experimental results.

Fig. 15 shows the experimental results. The left side shows the results obtained with the conventional method, and the right side shows those obtained with the proposed method. The results confirm that the proposed method suppresses FC-voltage fluctuation more effectively than the conventional method. Table IV summarizes the measured FC-voltage fluctuation. The proposed method reduces the normalized peak-to-peak FC-voltage fluctuation by 2.56 percentage points compared with the conventional method.

In addition, THD was calculated to evaluate the harmonic characteristics of the phase current and line-to-line voltage. The THD values up to the 2500th harmonic are listed in Table V, where the fundamental frequency is 50 Hz. Compared with the conventional method with the FC voltage set to 40% of the input voltage, the phase-current THD up to the 2500th harmonic remains almost unchanged, whereas the line-to-line-voltage THD slightly increases.

TABLE II. SIMULATION PARAMETERS.

System Parameter	Value
DC Voltage	DC 300 V
Flying Capacitor	1.8 mF
DC Link Capacitor	4.7 mF
Carrier Frequency	10 kHz
Resistance	5.5 Ω
Inductor	346 μH
Voltage Reference Frequency	50 Hz

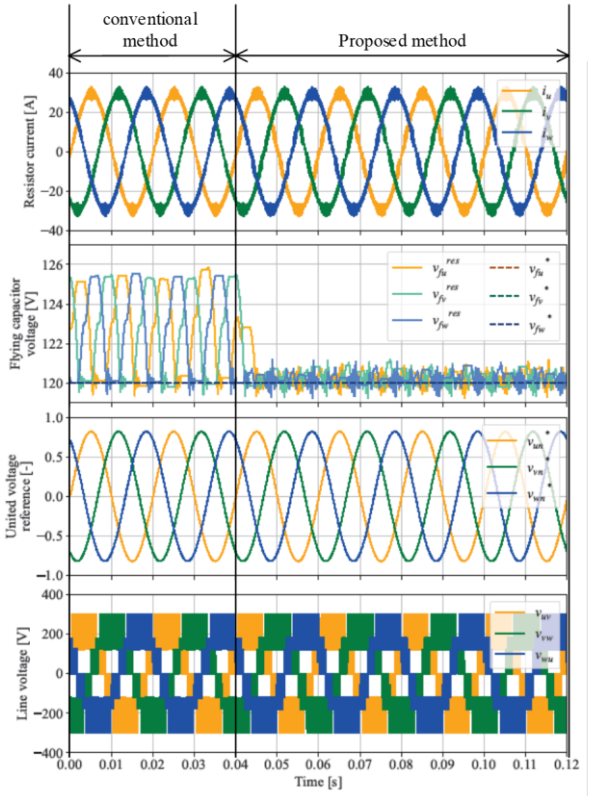

Fig. 13. Simulated Output Time Responses.

TABLE III. SIMULATED FC VOLTAGE FLUCTUATION.

method	Max FC Voltage [V]	Min FC Voltage [V]	FC Voltage Fluctuation [%]
conventional	125.7	119.2	5.42
proposed	121.3	119.2	1.75

The comparison was also made with the conventional method with the FC voltage set to 50% of the input voltage. The comparison results are shown in Fig. 16, and the corresponding THD values are also listed in Table V. In this case, the phase-current THD is reduced by 0.207 percentage points, and the line-to-line-voltage THD is reduced by 2.76 percentage points.

Furthermore, to examine the harmonic characteristics in more detail, frequency analysis up to 25 kHz was performed for the three methods described above. The results are shown in Fig. 17, and the phase-current amplitudes at the carrier-frequency component and its second harmonic are summarized in Table VI. The results indicate that the phase-

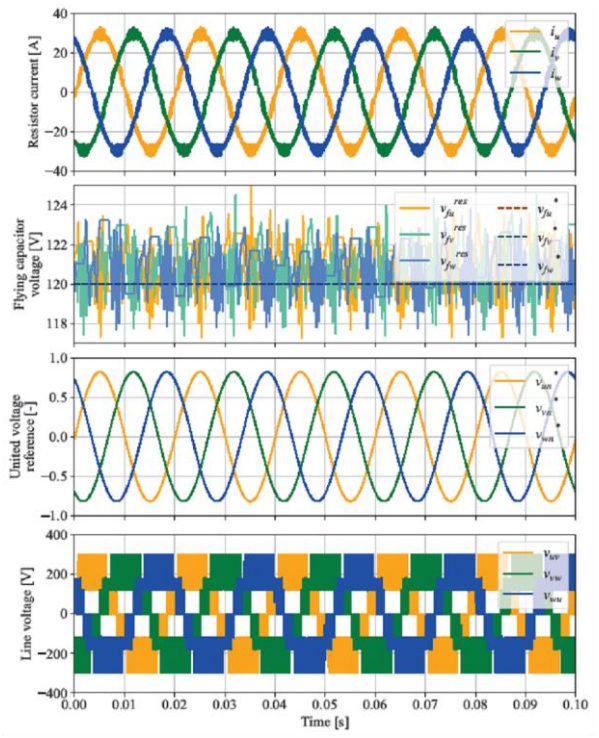

Fig. 14. Output Waveforms for Reduced FC Capacitance.

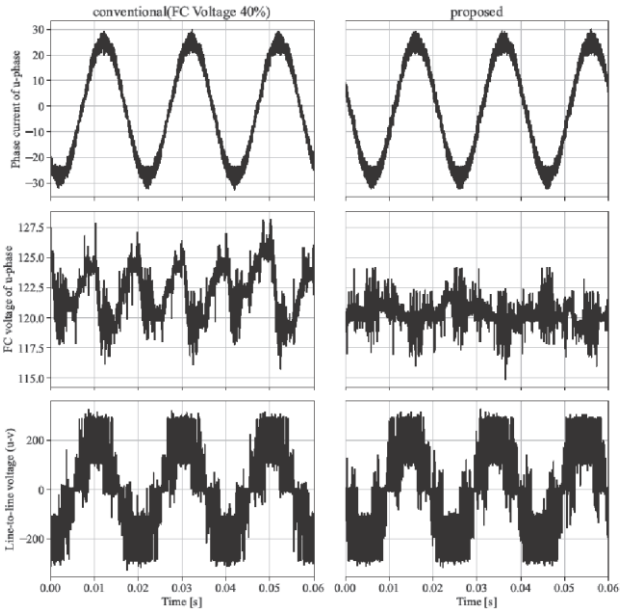

Fig. 15. Experimental Waveforms (Conventional 40% vs Proposed).

current amplitudes at the carrier-frequency component are almost identical for all three methods. However, at the second harmonic of the carrier frequency, the proposed method exhibits the smallest amplitude.

These results confirm that the proposed method is effective in suppressing FC-voltage fluctuation in the experiment as well. In the THD evaluation, the proposed method maintains characteristics comparable to those of the conventional method under the 40% condition, while THD reduction is observed in comparison with the conventional 50% condition.

VIII. SUMMARY

This paper proposes a space-vector modulation scheme for a 3+1-level flying-capacitor converter to reduce the required

TABLE IV. EXPERIMENTAL FC VOLTAGE FLUCTUATION

method	Max FC Voltage [V]	Min FC Voltage [V]	FC Voltage Fluctuation [%]
conventional	128.1	115.8	10.3
proposed	124.1	114.8	7.75

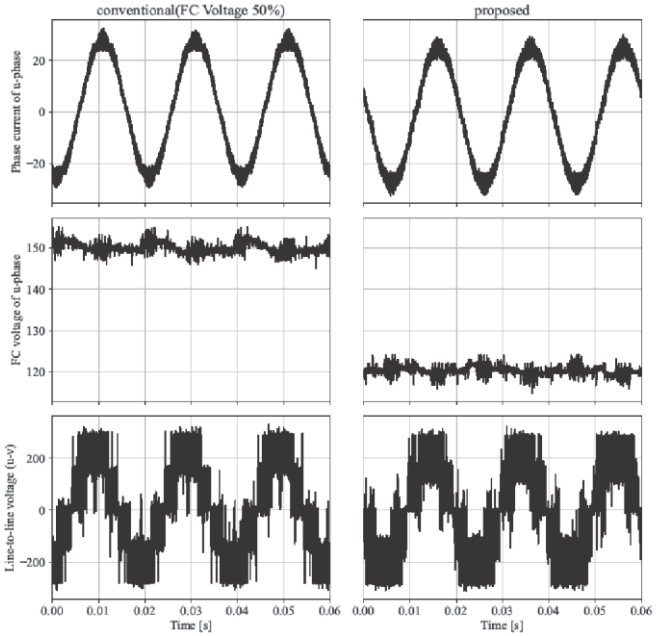

Fig. 16. Experimental Waveforms (Conventional 50% vs Proposed).

TABLE V. U-PHASE CURRENT/U-V LINE VOLTAGE THD (UNTIL 2500TH)

Quantity	Conventional (50%)	Conventional (40%)	Proposed
Phase current [%]	7.24	6.90	7.04
Line-to-line voltage [%]	35.6	31.8	32.9

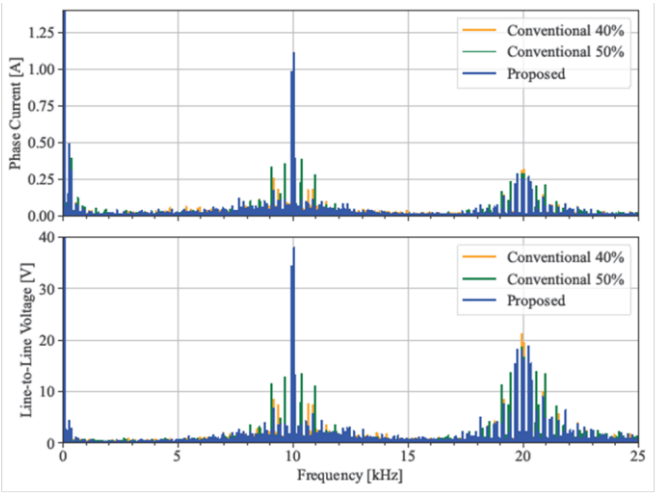

Fig. 17. Frequency Analysis Results (until 25 kHz).

TABLE VI. PHASE CURRENT AMPLITUDE.

Frequency	conventional (50%)	conventional (40%)	proposed
10 kHz	1.06	1.07	1.11
20 kHz	0.283	0.317	0.249

flying-capacitor capacitance. In the proposed method, both the maximum- and minimum-current phases are controlled, whereas the conventional method considers only the maximum-current phase. Simulation results showed that the FC voltage fluctuation rate was reduced to 1.75%, corresponding to a reduction of 3.67 percentage points, and that the required FC capacitance was reduced by 72.2% under the same voltage-fluctuation criterion. Experimental results also confirmed that the proposed method lowered the FC voltage fluctuation rate by 2.56 percentage points. In the THD evaluation, the proposed method maintained characteristics comparable to those of the conventional method under the 40% condition, while THD reduction was observed under the 50% condition. These results show that the proposed method effectively suppresses FC-voltage fluctuation while maintaining THD characteristics comparable to those of the conventional method, thereby demonstrating its practicality for reducing the required FC capacitance in 3+1-level FCCs.

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