Virtual Reactance Circuit for Miniaturizing the Grid-Side Inductor Based on Four-Terminal Network Theory

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***Abstract*—Improving the power density of power conversion systems (PCSs) requires reducing the size of passive components in grid-connected inverters. While increasing the switching frequency can reduce inductor size this approach may be impractical for high-power PCSs due to excessive switching losses and device limitations. This paper proposes a four-terminal virtual reactance circuit that emulates passive reactance behavior over a wide bandwidth while allowing only a small portion of the current to flow through its auxiliary circuit. The proposed topology is systematically described within the framework of four-terminal virtual reactance circuits based on four-terminal network theory. Its broadband characteristics are verified through simulation and experiment using an 800-W prototype. Furthermore, the total passive volume is reduced by 69% compared with a conventional passive inductor, demonstrating the effectiveness of the proposed circuit for passive component miniaturization in PCSs.**

Keywords—grid-connected inverter, grid-side inductor, virtual reactance circuit, four-terminal network theory

I. Introduction

In recent years, extensive research has focused on grid-connected inverters for photovoltaic (PV) systems [1–2]. Meanwhile, advances in digital control technology have enabled faster signal processing and more accurate current and voltage regulation [3]. To transfer power from PV systems to the utility grid, a power conversion system (PCS) is used. Increasing PCS power density requires downsizing the grid-side inductor, which occupies a large portion of the system volume [4–5]. In small- to medium-power PCS, this can be achieved by raising the inverter switching frequency; however, in high-power systems, increased switching losses and device limits restrict the allowable frequency [6].

As an alternative, virtual reactance circuits have been proposed to emulate inductive or capacitive characteristics by combining small passive components with switching converters [7–10]. These circuits can be connected in series or parallel, similar to passive components, and have been applied to reduce bulky passive elements in power converters. In [9], a virtual capacitor was implemented to replace the DC-link capacitor in a single-phase PV inverter. In addition, virtual inductors were implemented to replace DC-link or AC-side filter inductors in motor drives [10]. Virtual reactance circuits realize the desired reactance characteristics within their control bandwidth. However, conventional virtual reactance circuits are designed for relatively low-frequency applications and operate at switching frequencies of only a few kilohertz, thereby limiting their control bandwidth. As a result, they are not suitable for grid-connected inverters operating at several tens of kilohertz. Moreover, conventional circuits employ a two-terminal configuration, causing the entire line current to flow through the auxiliary circuit and increasing power losses.

To address these issues, a four-terminal virtual reactance circuit that significantly reduces the size of the grid-side inductor has been proposed [11]. In the proposed topology, the auxiliary circuit processes only the minimum current required to generate the desired virtual reactance, minimizing power loss and enabling higher switching-frequency operation. In [11], the proposed circuit was presented mainly as a specific topology for grid-side inductor miniaturization, and the volume evaluation focused on the inductors. In this paper, the proposed topology is described within the framework of four-terminal virtual reactance circuits based on four-terminal network theory. From this viewpoint, the proposed topology is understood as a realizable configuration of a four-terminal virtual reactance circuit, and its reactance characteristics are discussed in greater detail. In addition, the capacitor design and its volume evaluation are included, and the total passive volume is evaluated. Furthermore, a 69% reduction in total passive volume is achieved compared with a conventional inductor. The effectiveness of the proposed circuit and its design method is verified through simulations and experiments using an 800-W prototype.

II. Issues of Applying Conventional Virtual Reactance Circuits to Existing PCSs

Fig. 1 shows the concept of a conventional two-terminal virtual reactance circuit. In this approach, an integrator is used to generate the control reference for emulating inductive behavior. The virtual inductor can be modeled as

$$Z_{vir}(s) = \frac{v(s)}{i(s)} = sL_{vir} \tag{1}$$

where s is the Laplace operator.

According to (1), the command current $i_{cmd}(s)$ is obtained by sampling the terminal voltage $v(s)$, integrating it, and dividing by the desired inductance L_{vir}. The two-terminal structure can therefore reproduce the electrical characteristics of a passive inductor [7]. This configuration is envisioned as a direct replacement for passive inductors, allowing the downsizing of existing converter systems. Moreover, the

command inductance is dynamically tunable and maintains linearity within the control bandwidth of the virtual reactance circuit. Similarly, a virtual capacitor can be implemented by generating the command voltage so as to reproduce the electrical characteristics of a passive capacitor. Thus, a two-terminal virtual reactance circuit can emulate not only inductive behavior but also capacitive behavior within the control bandwidth.

Fig. 2 shows a practical configuration of a conventional two-terminal virtual reactance circuit. The circuit consists of passive components smaller than the desired virtual reactance and a controlled voltage source or controlled current source implemented by a high-frequency converter. Therefore, as long as sufficient control bandwidth is ensured, the desired reactance characteristics can be realized over a wide frequency range, including transient behavior.

From the viewpoint of network theory, a conventional two-terminal virtual reactance circuit constitutes a complete two-terminal network and can naturally be treated as equivalent to a single passive reactance element. However, in a two-terminal configuration, the current required to realize the emulated reactance is identical to the main-circuit current seen from the external terminals. Therefore, maintaining the desired reactance characteristics across the entire emulation bandwidth requires that virtual reactance operation be established for the full main-circuit current. When such a circuit is applied to an existing power converter, the virtual reactance operation is superimposed on the main-circuit current. As a result, the auxiliary circuit must handle a current comparable to the main-circuit current, thereby increasing circuit losses and hindering high power density. Furthermore, practical application to existing power converters requires the desired reactance characteristics to be maintained over a wide frequency range, including switching-frequency components, which in turn requires a high control bandwidth. Although increasing the switching frequency is effective for widening the control bandwidth, the two-terminal configuration tends to make the associated increase in circuit loss more pronounced, making broadband operation difficult.

III. Four-Terminal Virtual Reactance Circuit

To overcome the above limitation, a virtual reactance circuit is here considered as a four-terminal network in which the main-circuit operation of an existing power converter is separated from the virtual reactance operation. In this paper, this configuration is referred to as a four-terminal virtual reactance circuit, as opposed to the conventional two-terminal virtual reactance circuit.

A. Concept of the Four-Terminal Virtual Reactance Circuit

Fig. 3 shows the concept of the four-terminal virtual reactance circuit. Two basic circuits are introduced. The first is a voltage-source-type virtual reactance circuit, which consists of a shunt susceptance Y_{in} cascaded with a series voltage source $v_{aux}(t)$. The second is a current-source-type virtual reactance circuit, which consists of a series reactance Z_{in} cascaded with a shunt current source $i_{aux}(t)$.

From the viewpoint of network equivalence, circuits other than these basic configurations can be reduced to a series or parallel combination of Z_{in}, Y_{in}, and a virtual reactance, resulting in an equivalent reactance Z_{in}'. Therefore, realizable four-terminal virtual reactance circuits can be discussed starting from the two basic circuits shown in Fig. 3. These

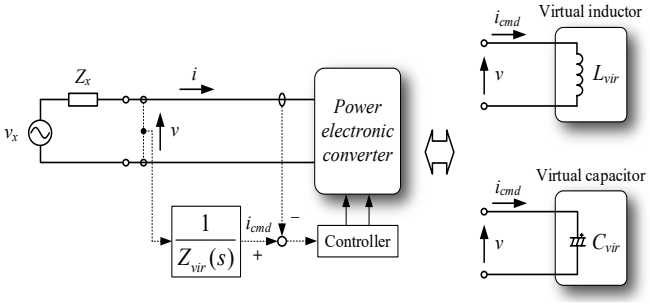


Fig. 1. Concept of the conventional two-terminal virtual reactance circuit.

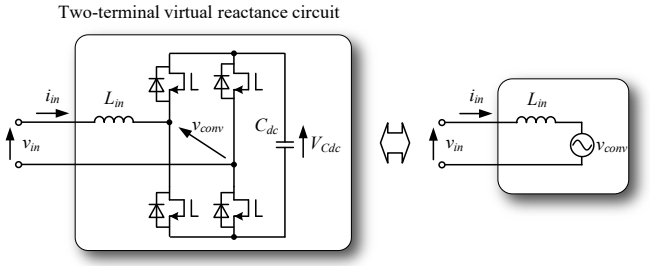
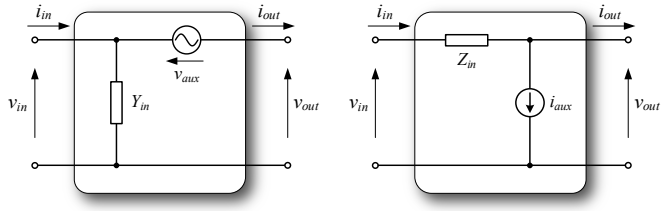
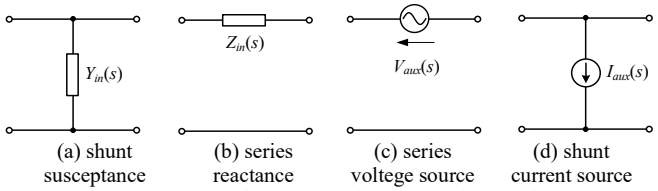


Fig. 2. Circuit configuration of a two-terminal virtual reactance circuit.



(a) voltage-source-type (b) current-source-type

Fig. 3. Concept of a four-terminal virtual reactance circuit.



(a) shunt susceptance (b) series reactance (c) series voltege source (d) shunt current source

Fig. 4. Basic elements of a four-terminal network.

circuits also include the conventional two-terminal virtual reactance circuit as a special case.

To analyze these circuits systematically, four-terminal network theory is introduced. In this paper, F-parameters are used because cascade connections of circuit elements can be represented by matrix multiplication. The F-parameter matrix $\boldsymbol{F}$(s) of a four-terminal network is defined by (2).

$$\begin{bmatrix} V_{in}(s) \\ I_{in}(s) \end{bmatrix} = \begin{bmatrix} A(s) & B(s) \\ C(s) & D(s) \end{bmatrix} \begin{bmatrix} V_{out}(s) \\ I_{out}(s) \end{bmatrix} = \boldsymbol{F}(s) \begin{bmatrix} V_{out}(s) \\ I_{out}(s) \end{bmatrix} \quad (2)$$

Fig. 4 shows the basic elements of the four-terminal virtual reactance circuit. To clarify the reactance characteristics of the basic circuits in Fig. 3, their F-parameters are derived. Because these circuits are expressed as cascade connections of the elements shown in Fig. 4, the F-parameters of the basic circuits are obtained as matrix products of the F-parameters of the individual elements. Therefore, the F-parameters of the shunt susceptance $Y_{in}(s)$, the series reactance $Z_{in}(s)$, the series voltage source $V_{aux}(s)$, and the shunt current source $I_{aux}(s)$ are first derived.

The F-parameters of $Y_{in}(s)$ and $Z_{in}(s)$, denoted by $\boldsymbol{F}_Y(s)$ and $\boldsymbol{F}_Z(s)$, are given by (3) and (4), respectively.

$$\boldsymbol{F}_Y(s) = \begin{bmatrix} 1 & 0 \\ Y_{in}(s) & 1 \end{bmatrix} \tag{3}$$

$$\boldsymbol{F}_Z(s) = \begin{bmatrix} 1 & Z_{in}(s) \\ 0 & 1 \end{bmatrix} \tag{4}$$

For $V_{aux}(s)$, KVL and current continuity give (5) and (6).

$$V_{in}(s) = V_{aux}(s) + V_{out}(s) \tag{5}$$

$$I_{in}(s) = I_{out}(s) \tag{6}$$

Here, $V_{aux}(s)$ is expressed as a linear combination of the terminal variables of the four-terminal network, as given by (7), so that the desired virtual reactance characteristics can be realized using only the terminal information.

$$V_{aux}(s) = a(s)V_{in}(s) + b(s)I_{in}(s) + c(s)V_{out}(s) + d(s)I_{out}(s) \tag{7}$$

From (5), (6), and (7), the F-parameter $\boldsymbol{F}_v(s)$ of the series voltage source is obtained as (8).

$$\boldsymbol{F}_v(s) = \begin{bmatrix} \dfrac{1+c(s)}{1-a(s)} & \dfrac{b(s)+d(s)}{1-a(s)} \\ 0 & 1 \end{bmatrix} = \begin{bmatrix} A_v(s) & B_v(s) \\ 0 & 1 \end{bmatrix} \tag{8}$$

Similarly, for $I_{aux}(s)$, KCL and voltage continuity give (9) and (10).

$$I_{in}(s) = I_{aux}(s) + I_{out}(s) \tag{9}$$

$$V_{in}(s) = V_{out}(s) \tag{10}$$

$I_{aux}(s)$ is also expressed as a linear combination of the terminal variables, as given by (11), and the F-parameter $\boldsymbol{F}_i(s)$ of the shunt current source is obtained as (12).

$$I_{aux}(s) = a(s)V_{in}(s) + b(s)I_{in}(s) + c(s)V_{out}(s) + d(s)I_{out}(s) \tag{11}$$

$$\boldsymbol{F}_i(s) = \begin{bmatrix} 1 & 0 \\ \dfrac{a(s)+c(s)}{1-b(s)} & \dfrac{1+d(s)}{1-b(s)} \end{bmatrix} = \begin{bmatrix} 1 & 0 \\ C_i(s) & D_i(s) \end{bmatrix} \tag{12}$$

Using (3), (4), (8), and (12), the F-parameters of the basic four-terminal virtual reactance circuits can be derived. The F-parameter of the voltage-source-type virtual reactance circuit $\boldsymbol{F}_V(s)$ is defined by (13), and that of the current-source-type virtual reactance circuit $\boldsymbol{F}_I(s)$ is defined by (14).

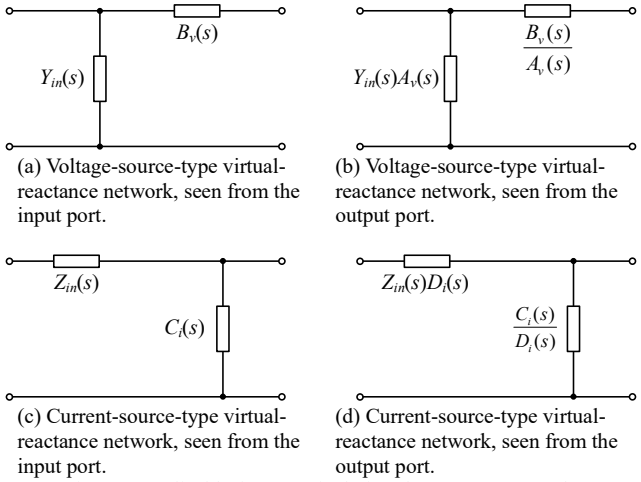
$$\boldsymbol{F}_V(s) = \boldsymbol{F}_Y(s)\boldsymbol{F}_v(s) = \begin{bmatrix} A_v(s) & B_v(s) \\ A_v(s)Y_{in}(s) & 1 + B_v(s)Y_{in}(s) \end{bmatrix} \tag{13}$$

$$\boldsymbol{F}_I(s) = \boldsymbol{F}_Z(s)\boldsymbol{F}_i(s) = \begin{bmatrix} 1 + C_i(s)Z_{in}(s) & D_i(s)Z_{in}(s) \\ C_i(s) & D_i(s) \end{bmatrix} \tag{14}$$

Thus, the basic four-terminal virtual reactance circuits can be represented systematically by the passive elements $Y_{in}(s)$ and $Z_{in}(s)$ and the control-dependent parameters $A_v(s)$, $B_v(s)$, $C_i(s)$, and $D_i(s)$.

B. Networks Realizable by the Four-Terminal Virtual Reactance Circuits

The realizable four-terminal virtual reactance networks can be clarified from the F-parameters of the basic circuits derived in the previous section. Fig. 5 shows the networks realizable by the four-terminal virtual reactance circuits. The networks realized by the circuits in Fig. 3 are not arbitrary four-terminal networks, but are restricted to a basic structure consisting of a cascade connection of one reactance element and one susceptance element. Representative realizable virtual reactance networks are described below.



(a) Voltage-source-type virtual-reactance network, seen from the input port.

(b) Voltage-source-type virtual-reactance network, seen from the output port.

(c) Current-source-type virtual-reactance network, seen from the input port.

(d) Current-source-type virtual-reactance network, seen from the output port.

Fig. 5. Realizable four-terminal virtual-reactance network.

In the voltage-source-type circuit, if $Y_{in}(s) = sC_{in}$ and the parameter $A_v(s)$ is controlled by the voltage source, a virtual capacitor $sC_{vir} = sA_v(s)C_{in}$ is realized at the output terminals, as shown in Fig. 5(b). Similarly, in the current-source-type circuit, if $Z_{in}(s) = sL_{in}$ and the parameter $D_i(s)$ is controlled by the current source, a virtual inductor $sL_{vir} = sD_i(s)L_{in}$ is realized at the output terminals, as shown in Fig. 5(d).

The four-terminal virtual reactance circuit can synthesize an equivalent reactance while separating the main-circuit operation from the virtual reactance operation. This is a distinctive feature of the four-terminal virtual reactance circuit. Furthermore, based on the F-parameters, the relationship between the voltage $V(s)$ and current $I(s)$ observed from the external terminals can be made equivalent to the terminal equation of the desired passive reactance element. Therefore, the resulting network is valid as a virtual reactance circuit.

IV. Proposed Virtual Reactance Circuit

A. Circuit Configuration

Fig. 6 illustrates a power conversion system (PCS) composed of a grid-connected inverter and a grid-side inductor. In high-power applications, the large passive inductor at the inverter output limits system downsizing. Increasing the switching frequency can reduce the inductor size, but this approach introduces higher switching losses and device constraints. To address this issue, this paper applies a four-terminal virtual reactance circuit to grid-side inductor miniaturization.

Fig. 7 shows the proposed four-terminal virtual reactance circuit. This circuit consists of two small inductors (L_{in}, L_f), a DC capacitor C_{dc}, and an H-bridge converter connected in parallel with the PCS output. From the viewpoint of the basic circuits discussed in the previous section, the proposed circuit is a practical realization of the current-source-type four-terminal virtual reactance circuit. This is because grid-side inductor miniaturization requires a large virtual inductor as seen from the output terminals, which can be realized by the

current-source-type circuit with $Z_{in}(s) = sL_{in}$ and the control parameter $D_i(s)$. Accordingly, the F-parameter of the proposed circuit, $\boldsymbol{F}_{pro}(s)$, is obtained from $\boldsymbol{F}_I(s)$ by setting $Z_{in}(s) = sL_{in}$ and is given by (15).

$$\boldsymbol{F}_{pro}(s) = \begin{bmatrix} 1 + sC_i(s)L_{in} & sD_i(s)L_{in} \\ C_i(s) & D_i(s) \end{bmatrix} \tag{15}$$

In this configuration, a large virtual inductor as seen at the output terminals, is realized via the control parameter $D_i(s)$, which is well-suited for grid-side inductor miniaturization. As a result, the proposed circuit can synthesize the desired virtual reactance while separating the main-circuit operation from the virtual reactance operation, thereby reducing power loss and enabling high-frequency operation with a wide control bandwidth. Consequently, bulky passive inductors in existing PCSs can be replaced by the proposed circuit.

B. Realization of the Desired Virtual Inductor

The control parameters $C_i(s)$ and $D_i(s)$ are determined through the regulation of the H-bridge converter current $I_{Lf}(s)$. According to (2), (15), and KCL, $I_{Lf}(s)$ should be controlled as follows:

$$I_{Zvir,cmd}(s) = \left[1 - \frac{1}{D_i(s)}\right] I_{in}(s) + \frac{C_i(s)}{D_i(s)} V_{out}(s) \tag{16}$$

Thus, by regulating $I_{Lf}(s)$ according to this expression, the proposed circuit can emulate the desired virtual four-terminal reactance network.

To satisfy grid current harmonic constraints defined by standards such as IEEE 1547 [12], the proposed circuit must present a sufficiently large virtual inductor $L_{vir,grid}$ at the grid side. Therefore, the control parameters $C_i(s)$ and $D_i(s)$ should be set as follows:

$$C_i(s) = 0, \quad D_i(s) = N_{vir} = L_{vir,grid} / L_{in} \tag{17}$$

Based on KCL and (16), (17), the input current $I_{in}(s)$ and the inductor current $I_{Lf}(s)$ can be expressed as

$$I_{in}(s) = N_{vir} I_{out}(s), \quad I_{Lf}(s) = \left[N_{vir} - 1\right] I_{out}(s) \tag{18}$$

To achieve inductor miniaturization, the proposed circuit is typically designed such that $N_{vir} >> 1$. However, when a large linear inductance $L_{vir,grid}$ is implemented over the entire control bandwidth, both the grid-connected inverter and the H-bridge converter must handle significantly larger currents than in normal operation, thereby increasing power losses.

To address these issues, the proposed circuit emulates a nonlinear virtual inductor $L_{vir}(s)$ expressed as follows:

$$L_{vir}(s) = \left[L_{vir,grid} - L_{in}\right] \frac{s^2 + d \cdot 2\zeta\omega_{out}s + \omega_{out}^2}{s^2 + 2\zeta\omega_{out}s + \omega_{out}^2} + L_{in} \tag{19}$$

In this approach, $D_i(s)$ is controlled in real time so that $L_{vir}(s)$ behaves as a small inductance L_{in} around the grid frequency ω_{out}, while a much larger inductance $L_{vir,grid}$ is emulated at other frequencies. This configuration enables accurate emulation of the desired inductance characteristics while effectively reducing power losses in the system.

Fig. 8 shows the control block diagram of the proposed four-terminal virtual reactance circuit [11]. The control consists of two main paths. The first path generates the command current $i_{Zvir,Lf}$ to realize the desired four-terminal virtual reactance characteristics. The second path generates a control current i_{Rvir} to regulate the DC capacitor voltage v_{Cdc} and maintain stable operation of the auxiliary circuit [13–14]. These two currents are summed to form the total control current $i_{Lf,cmd}$, which is used in a closed-loop inductor current controller to generate the H-bridge converter voltage command $v_{H\text{-}bridge,cmd}$ for PWM modulation.

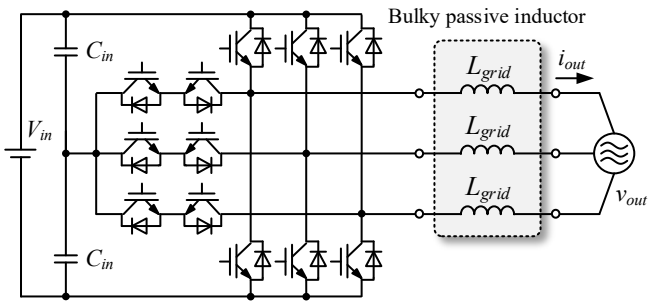


Fig. 6. A typical high-power grid-connected inverter.

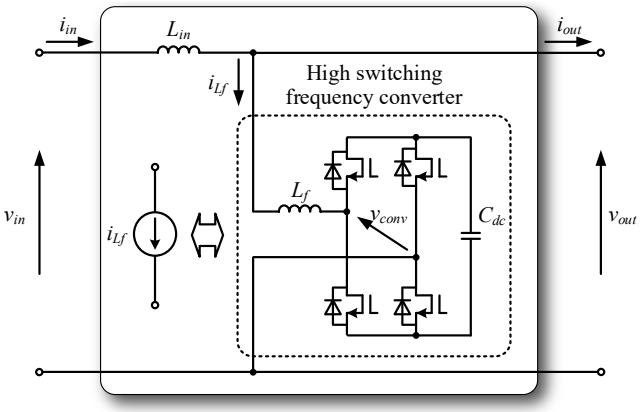


Fig. 7. Proposed four-terminal virtual reactance circuit.

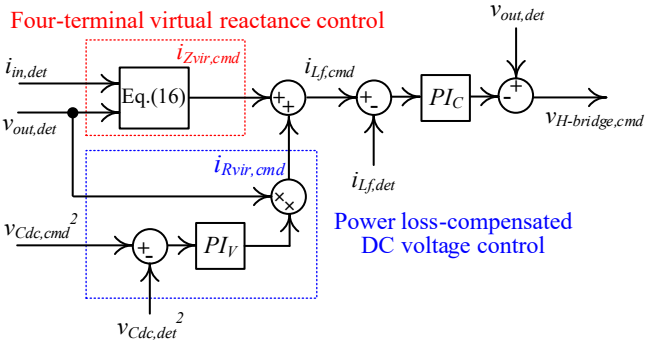


Fig. 8. Control block diagram of the proposed virtual reactance circuit.

C. Estimation of Inductor and Capacitor Volume

In this section, the design of the inductor and capacitor in the proposed circuit is presented. The circuit is assumed to emulate the virtual inductor defined by (19). The output current $i_{out}(t)$ includes the high-frequency ripple component of $i_{Lf}(t)$, which is generated by the H-bridge converter. The average voltage $V_{H\text{-}bridge}$ across the output terminal of the H-bridge converter, taken over one carrier cycle of the grid-connected inverter, can be expressed as follows.

$$V_{H\text{-}bridge} = \left[1 + \frac{L_f}{L_{in}} \alpha_L\right] V_{out,max}, \quad \alpha_L = 1 - \frac{1}{N_{vir}} \tag{20}$$

TABLE I. SIMULATION AND ANALYSIS PARAMETERS

Parameters of the grid-connected inverter		
Output power	P_{out}	1 kW
Input voltage	V_{in}	400 V
Output voltage	V_{out}	100 V_{rms}
Output frequency	f_{out}	50 Hz
Switching frequency	f_{inv}	10 kHz
Current ripple ratio of i_{out}	ΔI_{out}	10 %
Parameters of the proposed virtual reactance circuit		
Average voltage of C_{dc}	V_{Cdc}	300 V
Voltage ripple ratio of v_{Cdc}	ΔV_{Cdc}	5 %
Switching frequency	$f_{H\text{-}bridge}$	1 MHz

The inductance L_f is calculated from the high-frequency current ripple $\Delta I_{Lf,h}$ and the voltage $V_{H\text{-}bridge}$.

$$L_f = \frac{V_{out,max} L_{in} \left[V_{Cdc} - V_{out,max} \right]}{2 f_{H\text{-}bridge} \Delta I_{Lf,h} V_{Cdc} L_{in} - \alpha_L V_{out,max} \left[V_{Cdc} - V_{out,max} \right]} \quad (21)$$

where V_{Cdc} is the average voltage of C_{dc}, and $f_{H\text{-}bridge}$ is the switching frequency of the H-bridge converter. The output current ripple requirement ΔI_{out} is regulated by the grid code. The inductance $L_{vir,grid}$ is selected such that the total output current ripple, including the high-frequency current ripple caused by $i_{Lf}(t)$, does not exceed this limit.

$$L_{vir,grid} = \frac{V_{in} - V_{out,max}}{2 f_{inv} \left[\Delta I_{out} - \Delta I_{Lf,h} \right]} \frac{V_{out,max}}{V_{in}} \quad (22)$$

Where V_{in} and f_{inv} denote the input voltage and the switching frequency of the grid-connected inverter, respectively. The inductance L_{in} is determined from the current ripple ΔI_{in}.

$$L_{in} = \frac{V_{in} - V_{out,max}}{2 f_{inv} \Delta I_{in}} \frac{V_{out,max}}{V_{in}} \quad (23)$$

The DC capacitor voltage $v_{Cdc}(t)$ pulsates at twice the grid frequency ω_{out} due to the third-harmonic component of the grid-connected inverter current, which is the main component of the emulated virtual inductor current. Therefore, the capacitance C_{dc} is designed based on the voltage ripple ΔV_{Cdc}, as expressed by the following equation.

$$C_{dc} = \frac{3 V_{out,max} I_{3,max}}{4 \omega_{out} V_{Cdc} \Delta V_{Cdc}} \frac{N_{vir} - 1}{N_{vir}} \quad (24)$$

V. SIMULATION AND EXPERIMENTAL RESULTS

A. Passive Component Volume Estimation Results

Table I summarizes the simulation and analysis parameters. The inductor volume was calculated using the Area Product method [15–16], and the capacitor volume was estimated from a datasheet conversion factor [17]. As shown in Fig. 9, the experimental results agree well with the design points, confirming the validity of the volume estimation. The total passive volume was reduced by up to 69% compared

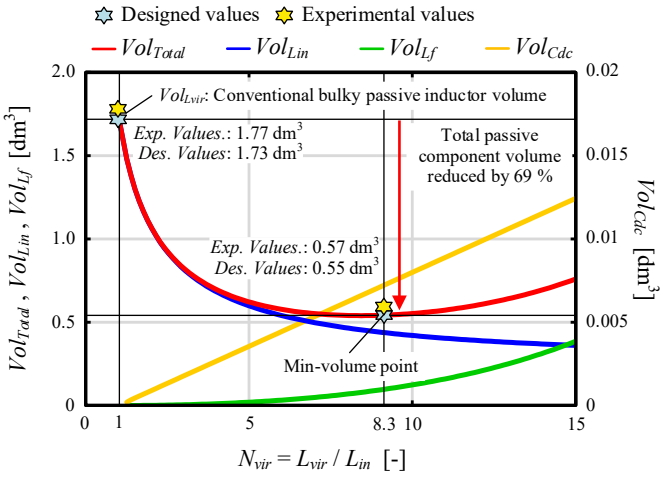


Fig. 9. Calculated and experimental passive component volumes.

TABLE II. EXPERIMENTAL PARAMETERS

Parameters of the grid-connected inverter		
Output power	P_{out}	800 W
Input voltage	V_{in}	380 V
Output voltage	V_{out}	200 V_{rms}
Output frequency	f_{out}	50 Hz
Switching frequency	f_{inv}	5 kHz
Current ripple ratio of i_{out}	ΔI_{out}	20 %
Inductance of a virtual inductor	$L_{vir,grid}$	12 mH (%Z = 7.5 %)
Parameters of the proposed virtual reactance circuit		
Average voltage of C_{dc}	V_{Cdc}	380 V
Switching frequency	$f_{H\text{-}bridge}$	150 kHz
Inductance of L_{in}	L_{in}	3 mH (%Z = 1.8 %)
Inductance of L_f	L_f	500 μH (%Z = 0.3 %)

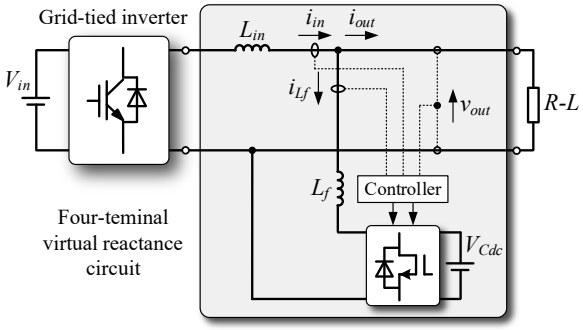


Fig. 10. Grid-tied inverter using the proposed circuit.

with a conventional inductor, and the simulated voltage and current ripples satisfied the design targets.

B. Experimental Results

An 800-W two-level single-phase grid-tied inverter is used to examine the basic operation of the proposed four-terminal virtual reactance circuit. Fig. 10 shows the experimental configuration, and Table II summarizes the parameters. In this setup, the bulky passive inductor $L_{vir,grid}$ is replaced by the proposed virtual reactance circuit. The virtual inductance is evaluated from the current ripple. To simplify the evaluation, the grid-tied inverter is operated in open-loop control with an RL load, and a DC power supply is used in place of the capacitor C_{dc} in the proposed circuit.

Fig. 11 shows the measured waveforms with the proposed virtual reactance circuit. In the proposed circuit, the target virtual inductance $L_{vir,grid}$ is determined on the basis of the small inductor L_{in}, and the current i_{Lf} appears as the high-frequency ripple current required to realize the corresponding F-parameters. In this experiment, L_{in} was set to 3 mH, whereas the target virtual inductor was set to 12 mH, which corresponds to the inductance required to achieve an output current ripple ratio of 20%. Before virtual reactance control, the output current ripple was 2.98 A. After the control was activated, the ripple decreased to 0.81 A, which corresponds to the target ripple ratio of approximately 20%. These results confirm that the proposed circuit successfully realizes the target virtual inductance.

VI. Conclusion

This paper presented a four-terminal virtual reactance circuit for miniaturizing the grid-side inductor in grid-connected inverters. The proposed topology was described within the framework of four-terminal virtual reactance circuits based on four-terminal network theory and was positioned as a practical realization of the current-source-type basic circuit. Based on this viewpoint, the reactance characteristics of the proposed circuit were clarified systematically, and the passive component design method, including both the inductors and the DC capacitor, was presented. The passive component volume was evaluated, and the total passive volume was reduced by 69% compared with a conventional passive inductor. In addition, experiments using an 800-W prototype confirmed that the proposed circuit successfully realizes the target virtual inductance and achieves the desired output current ripple. Therefore, the proposed circuit is effective for replacing bulky passive inductors in existing PCSs and is promising for realizing high-power-density grid-connected inverters.

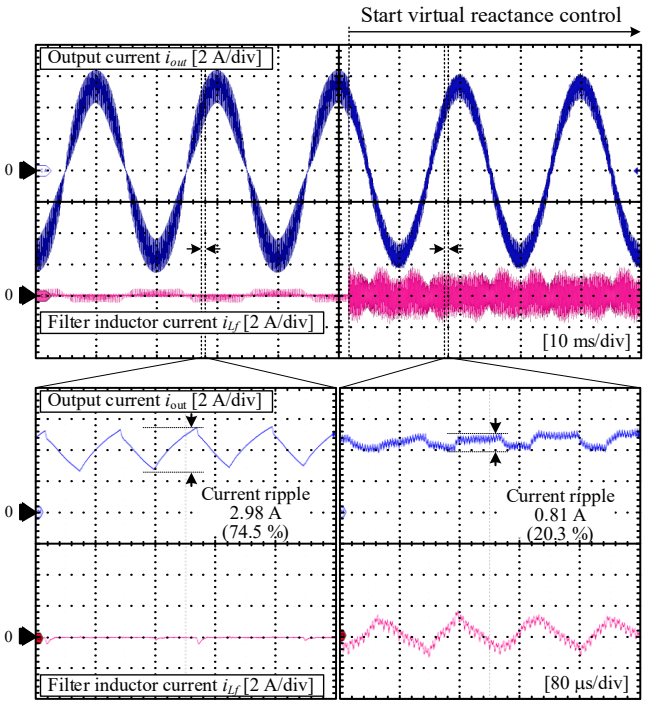


Fig. 11. Experimental results of the proposed circuit.

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