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Improvement of self-resonant frequency in a multilayer PCB planar inductor through winding layout modification

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Abstract The growing demand for high-efficient power systems has driven the development of high-frequency passive components, including passive inductors. In this paper, multilayer printed circuit board (PCB) inductor, a type of inductor with excellent high-frequency characteristics that can be obtained through well-designed geometry arrangement, is investigated. Then a method to improve the frequency characteristics is introduced. By alternating the trace width value of the coil, the turn-to-turn parasitic capacitances between traces are reduced with little effect on the inductance value, through which the self-resonant frequency (SRF) of the PCB inductor is increased. The effectiveness of the proposed method is verified experimentally and reported herein.

Key words multilayer PCB inductor, frequency characteristic, parasitic capacitance, octagonal coil, trace width decrement

1. Introduction

Industrial growth and rapid expansion of data centers around the world have significantly increased the energy consumption, especially the electricity demand. At the same time, as electrification is widely recognized as an alternative to fossil fuels in the effort to reduce the greenhouse effect and carbon dioxide emissions, future consumption of electricity is expected to rise further. To meet these demands, highly efficient power conversion circuits capable of high power density and compact size are required. Recent advances in wide-bandgap active power devices (SiC, GaN) have enabled such circuits to operate at higher switching frequencies, but the realization of highly efficient power systems is not solely dependent on active devices. Therefore, many efforts have been made to improve the frequency characteristics of a circuit's passive components.

Passive inductors, an important component of power conversion circuits, are highly sensitive to high-frequency operation. Their inductive behavior can easily be altered by the parasitic components, leading to degraded performance and significantly affecting the whole power system. As a result, much research on the topic of enhancing passive inductors' frequency characteristics has been carried out, contributing greatly to the development of not just high-frequency inductors but also high-efficient power systems.

Printed circuit board (PCB) inductors, a type of inductor that is directly fabricated on a PCB, offer many advantages, including geometric precision, mechanical stability, and miniaturization, and are gaining attention as one of the promising high-frequency passive inductors for applications such as power converters, EMI filters, and RF circuits. However, their characteristics are greatly influenced by winding layout, board material, and even parasitic effects such as mutual capacitance, turn-to-turn parasitic capacitance, limiting their high-frequency performance and affecting their self-resonant frequency. In this paper, a method to mitigate the parasitic

capacitance of multilayer PCB inductors and enhance the self-resonant frequency is presented, verified experimentally, and reported herein.

2. Introduction and modeling of a multilayer PCB inductor

In this paper, the effectiveness of the proposed method for reducing parasitic capacitance is verified using multilayer PCB planar inductors with a simple octagonal spiral pattern. Specifically, a 2-layer and a 3-layer PCB inductor with the layouts as shown in Fig. 1 are utilized, and their design parameters are presented in Table 1. The multilayer structure is achieved by stacking up the corresponding number of single-layer PCB inductors and connecting them in series, as depicted in Fig. 1(c). In this work, layers of PCB inductor are arranged closely so that the distance between layers h_l is the substrate FR4 thickness h_{FR4}.

Using paper [1] as a reference, basic calculations of inductance L_s, series resistance R_s, parasitic capacitance between traces C_p, and PCB substrate parasitic components of C_{FR4} and R_{FR4} of a single-layer PCB planar inductor can be obtained. Therefore, only parameters related to the multilayer characteristics of PCB inductors are discussed herein. As mentioned in [1], the inductance of the PCB inductor is calculated using the modified Wheeler formula for a single-layer octagonal spiral inductor. However, stacking up layers of PCB inductors creates mutual coupling between the layers, as a result, the inductance formulas for 2-layer and 3-layer PCB inductors, assuming the self-inductance of each layer is equal to L_s, are as follows:

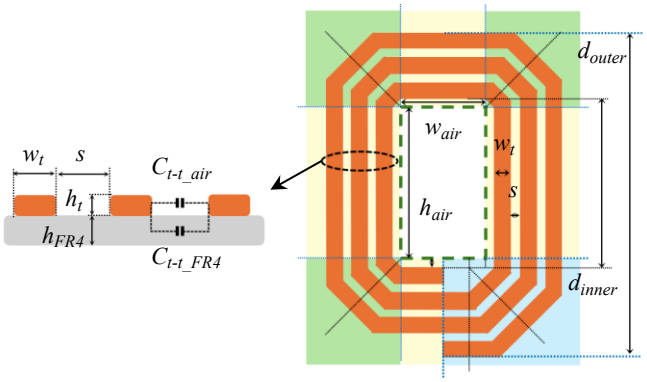
$$L_s = 2.25 \times \mu_0 \times \frac{n^2 \times d_{avg}}{1 + 3.55 \times \emptyset} \quad (1)$$

$$L_{2\text{-}layer} = 2 \times L_s + 2 \times M_{12} = 2 \times L_s + 2 \times k_{12} \times L_s \quad (2)$$

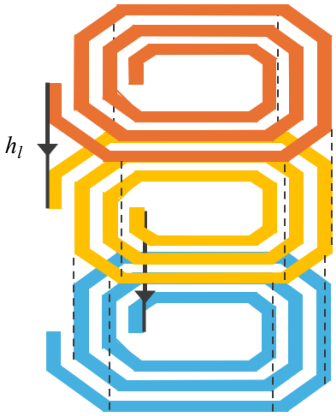
$$L_{3\text{-}layer} = 3 \times L_s + 2 \times M_{12} + 2 \times M_{13} + 2 \times M_{23}$$
$$= 3 \times L_s + 2 \times L_s \times (k_{12} + k_{13} + k_{23}) \quad (3)$$

with M is the mutual inductance between layers and k is the coupling coefficient.

Because the PCB inductor layers are stacked up and connected in series, the total series resistance of m-layer PCB inductors can easily be calculated as:



(a) Cross-sectional view (b) Top view



(c) Side view (3-layer PCB inductor)

Fig. 1. PCB inductor layout.

Table 1. Design parameters.

Parameter	Symbol	Value	Unit
Trace width	w_t	0.0015	m
Trace spacing	s	0.0015	m
Air core width	w_{air}	0.008	m
Air core height	h_{air}	0.014	m
Inner diameter (vertical)	d_{inner}	0.02	m
Outer diameter (vertical)	d_{outer}	0.098	m
Copper thickness	h_t	35×10^{-6}	m
Substrate FR4 thickness	h_{FR4}	0.001565	m
PCB thickness	h_{PCB}	0.0016	m
Distance from air core to the neareast turn	a	0.003	m
Number of turns	n	13	
Number of layers	m	2 or 3	
Copper resistivity	ρ_{Cu}	1.7×10^{-8}	Ωm
Copper relative permeability	μ_{r_Cu}	1	
FR4 dielectric permittivity	ε_{r_FR4}	4.4	
FR4 volume resistivity	ρ_{FR4}	10^{13}	Ωm
Vacuum permittivity	ε_0	8.854×10^{-12}	F/m
Vacuum permeability	μ_0	$4\pi\times10^{-7}$	H/m

$$R_{m\text{-}layer} = m \times R_s \quad (4)$$

Next, the parasitic capacitance of a multilayer PCB inductor is discussed. In a simple single-layer planar PCB inductor, the main parasitic components include stray capacitance from the trace through the substrate to ground C_{FR4} and turn-to-turn parasitic capacitance between traces C_p, which consists of parasitic capacitance through a dielectric layer of air $C_{t\text{-}t\_air}$ and through a dielectric layer of PCB substrate FR4 $C_{t\text{-}t\_FR4}$. However, when many layers of PCB inductor are arranged on top of each other, the well-overlapped traces between them form a parallel plate capacitor, which is the additional parasitic capacitance between layers in a multilayer PCB inductor. The better the coils overlap, the larger this mutual capacitance becomes. Calculations of the explained parameters are expressed as follows:

$$C_p = C_{t\text{-}t\_air} + C_{t\text{-}t\_FR4} = (1 + \varepsilon_{r\_FR4}) \times \varepsilon_0 \times \frac{h_t \times l}{s} \quad (5)$$

$$C_{FR4} = \frac{1}{2} \times \varepsilon_0 \times \varepsilon_{r\_FR4} \times \frac{l \times w_t}{h_{FR4}} \quad (6)$$

$$C_{layer12} = \varepsilon_0 \times \varepsilon_{r\_FR4} \times \frac{l \times w_t}{h_l} = 2 \times C_{layer13} \quad (7)$$

From the above formulas, theoretical models of a 2-layer and a 3-layer PCB inductor are established. Using frequency characteristics experimental results of the PCB inductor in Table 1 for verification, a comparison of inductance and self-resonant frequency between theoretical model calculations and experimental values was performed and demonstrated in Table 2. The results show that the model predictions are in good agreement with real-life PCB inductor characteristics.

3. Improvement of self-resonant frequency in a multilayer PCB inductor through parasitic capacitance reduction

This paper proposes a method to improve the frequency characteristics of a multilayer PCB inductor by increasing the self-resonant frequency through a technique that reduces parasitic capacitance. As explained above, the parasitic capacitances of a multilayer PCB inductor include the turn-to-turn parasitic components between traces, the mutual capacitance between layers,

Table 2: Comparison between theoretical calculation and experimental result for 2-layer and 3-layer PCB inductor.

2-layer PCB inductor	Theoretical calculation	Experimental result	Error [%]
Inductance [uH]	32.01	29.30	8.47
SRF [MHz]	3.72	3.81	2.36
3-layer PCB inductor	Theoretical calculation	Experimental result	Error [%]
Inductance [uH]	66.55	63.1	5.18
SRF [MHz]	2.92	2.94	0.72

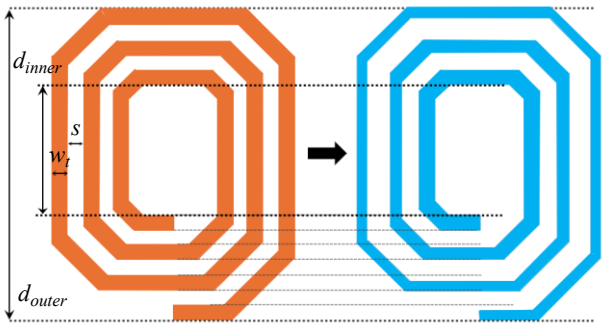


Fig. 2. Visualization of trace width decrement method.

and the PCB substrate parasitic capacitance. As seen from formulas (5), (6), and (7), these parasitic capacitances can be mitigated by optimizing the trace width and trace spacing of the inductor coil. By reducing the trace width or widening the trace spacing, a decrease in parasitic capacitance can be expected.

It is also necessary to maintain the inductance value while reducing parasitic components; therefore, variables that affect the outcome of the inductance formula will be discussed. From the above formulas (2) and (3), it can be concluded that the self-inductance and the coupling coefficient between each layer of the PCB inductor are responsible for any changes in the inductance result. The coupling coefficient is a parameter that represents how strongly the magnetic flux from one inductor links with the other,and is generally affected by the distance between two inductors, coil alignment, board material, etc. In this paper, the distance between PCB layers is fixed, minimizing the effect on the total inductance result. The second variable – the self-inductance of each layer of PCB inductor – is determined by the modified Wheeler formula (1), in which four noticeable factors could affect the inductance: the

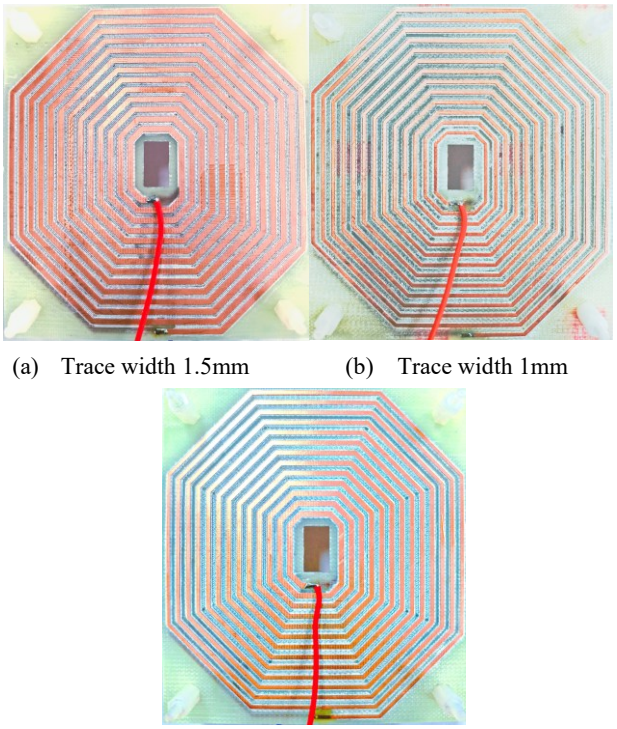
geometric coefficients, the number of turns, and the inner and outer diameter of the spiral coil. These parameters are all related to the shape of the PCB inductor coil, so the inductance value can be maintained if the overall shape of the octagonal spiral coil remains unchanged.

From the above analysis, self-resonant frequency is expected to be improved by applying methods that reduce the most significant parasitic component – parasitic capacitance between layers of a multilayer PCB inductor. The proposed method is based on two conditions: targeting the reduction of layer-to-layer parasitic capacitance and maintaining the inner and outer diameters of the spiral coil to mitigate the effect on inductance. From the capacitance formula, it is confirmed that the parasitic component reduced without affecting the inductance by narrowing the PCB inductor's trace width. However, there is one drawback of a narrow coil's trace width: the smaller the trace width is, the larger the DC resistance becomes . With a limited area confined by the inner and outer diameters of the coil and the unwanted effect of a narrow trace width, a trace width decrement method across the number of turns is proposed and tested.

3.1. Effect of trace width decrement on multilayer PCB inductor frequency characteristics.

Based on the above analysis, this paper proposes a method that reduces the parasitic capacitance with little effect on inductance: from the inner loop toward the outer loop of the inductor coil, the trace width will gradually be narrowed until a specific value. This specific value is determined based on design conditions such as PCB fabrication limitations, current density minimum requirements, etc. Because the PCB space is limited by the inner and outer diameter of the coil, by reducing the trace width of PCB inductor from the inner toward the outer loop, the trace spacing will also be increased correspondingly, as illustrated in Fig. 2. Supposed that the inner trace width is A [mm], the outer specified trace width is B [mm] and the number of layers is m, the amount of trace width reduced after every loop is calculated as $(A - B) / (m - 1)$ [mm].

To verify the effectiveness of the described method, three PCB inductors with different trace widths, as shown in Fig. 3, were fabricated. Fig. 3(a) is the PCB inductor with uniform trace width and trace spacing of 1.5mm, while the one in Fig. 3(b) has a trace width of 1mm and trace spacing of 2mm. The proposed method is realized in the PCB inductor in Fig. 3(c), where the inner loop's trace width of 1.5mm will gradually be reduced to 1mm after 13 turns. The experiment was conducted for both 2-layer and 3-layer PCB inductors, and the results are summarized in Table 3. For a 2-layer



(a) Trace width 1.5mm (b) Trace width 1mm

(c) Trace width reduction: 1.5mm to 1mm (Inner to outer)

Fig. 3. PCB inductors with different trace widths.

Table 3: Comparison between different trace widths for 2-layer and 3-layer PCB inductors.

2-layer PCB inductor			
Parameter / Case	Inductance [uH]	SRF [MHz]	DC resistance [Ω]
1.5mm	29.3	3.81	1.73
1mm	29.5	4.28	2.6
1.5mm to 1mm	30.0	3.96	2.25

3-layer PCB inductor			
Parameter / Case	Inductance [uH]	SRF [MHz]	DC resistance [Ω]
1.5mm	63.1	2.94	2.64
1mm	63.8	3.20	3.89
1.5mm to 1mm	64.0	3.03	3.27

PCB inductor, the inductances between the three cases are slightly different, with the most significant deviation of about 2.39%. Compared to the 1.5-mm trace-width PCB inductor, the proposed inductor helps increase the self-resonant frequency by approximately 3.84%. When the whole trace width is 1mm, the increased SRF resulting from the proposed method is relatively small, but it helps lower DC resistance by up to 13.46%. The same pattern is observed for the results of a 3-layer PCB inductor. With a maximum relative inductance difference of about 1.43%, the proposed method increases the SRF by about 2.86% and decreases the DC resistance by up to 16%, compared to 1.5-mm- and 1-mm-wide trace-width 3-layer PCB inductors, respectively. In conclusion, the proposed trace width decrement method is effective in increasing the self-resonant frequency of a multilayer PCB inductor while lowering the amount of DC resistance increased when the trace width is too narrow.

3.2. Combined effect of trace width decrement and elimination of PCB substrate between traces

The trace-width-decrement method aims to reduce parasitic capacitance between layers of a multilayer PCB inductor and between traces on each layer by gradually decreasing the trace width from the inner loop toward the outer loop. Additionally, based on [1], the turn-to-turn parasitic capacitance can be further reduced by applying the method of eliminating the PCB substrate between traces. The working principle of this method is simple and explainable using the turn-to-turn parasitic capacitance formula (5). As written in the equation, the parasitic capacitance between traces, consisting of capacitances that take air and PCB substrate as dielectric layer, is significantly influenced by the dielectric permittivity of the substrate. In this work, the PCB substrate material is FR4, which has a dielectric permittivity 4 times that of air, contributing significantly to the total parasitic capacitance. [1] suggested a simple method of drilling holes between the traces to eliminate the high-permittivity material, thereby reducing the overall turn-to-turn parasitic capacitance. The method is applicable to all PCB materials, as their permittivity are always greater than that of air. However, this method has a small drawback: a complete elimination of PCB substrate between traces is impossible as it would cause the whole structure to collapse; and therefore, small bits of substrate are left at the corners for stability purposes. These small residual PCB substrates unexpectedly reduce the effectiveness of the method, as explained in [1].

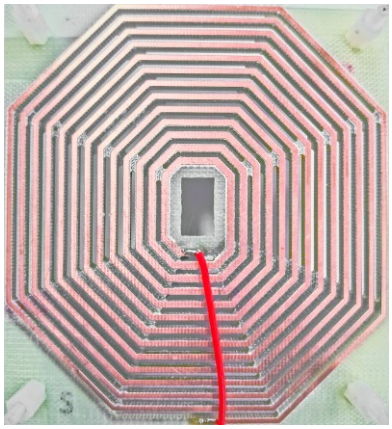


Fig. 4. Combined application of trace width decrement and PCB substrate elimination.

Table 4: Comparison with and without PCB substrate elimination for 2-layer and 3-layer PCB inductors.

2-layer PCB inductor			
Parameter / Case	Inductance [uH]	SRF [MHz]	DC resistance [Ω]
Without hole	30.0	3.96	2.25
With hole	29.5	4.22	2.31

3-layer PCB inductor			
Parameter / Case	Inductance [uH]	SRF [MHz]	DC resistance [Ω]
Without hole	64.0	3.03	3.27
With hole	63.4	3.24	3.41

In this section, to verify the combined effect of both methods, the proposed trace width decrement method as in Fig. 3(c) is realized in combination with the elimination of PCB substrate between traces, and the fabricated PCB inductor is shown in Fig. 4. The experiment was also conducted for both 2-layer and 3-layer PCB inductors, and the results of inductance and SRF with and without holes between coil traces are summarized in Table 4. The results of the multilayer PCB inductor without drilling holes are equal to the results of the PCB inductor with a trace width that decreases from 1.5mm to 1mm

in Table 3. For a 2-layer PCB inductor, when applying the PCB substrate elimination method, a small deviation of about 1.67% in inductance is observed, along with a 6.66% increase in SRF and an unwanted 2.67% increase in DC resistance. The same pattern in the results is also recorded for a 3-layer PCB inductor, with inductance deviation of 0.94%, an increase of about 7% and 4.28% in SRF and DC resistance, respectively. This outcome proves that when combining the trace width decrement and PCB substrate elimination methods together, parasitic capacitance can further be reduced, resulting in an increase in SRF and unwanted DC resistance. When comparing the PCB inductor using both the trace width decrement and PCB substrate elimination method with the 1.5-mm and 1-mm trace-width-PCB inductors, a significant increase in SRF up to 10% is observed with smaller DC resistance in both cases of 2-layer and 3-layer PCB inductors.

4. Conclusion

This paper proposes a method of alternating the trace width of the inductor spiral coil to reduce the turn-to-turn parasitic capacitance and the mutual capacitance between layers, aiming to improve the self-resonant frequency of a multilayer PCB planar inductor. From the inner loop toward the outer loop of the inductor coil, the trace width is gradually narrowed to a specific value while time enlarging the trace spacing between outer loops. The proposed method was applied to 2-layer and 3-layer PCB inductors, and the results showed that it is effective in increasing the SRF while maintaining an equal inductance and a smaller DC resistance compared to PCB inductors with a consistent trace width. Furthermore, the proposed trace width decrement method can be used in combination with the PCB substrate elimination method, resulting in a significant increase in SRF with DC resistance remaining smaller than narrow-trace-width multilayer PCB inductors.

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