Design of ZVS Inductor Considering Load Power Factor Variations in a ZVS Tank Inverter

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Abstract - High-frequency inverters are commonly employed in induction heating and wireless power transfer, where achieving zero-voltage switching (ZVS) is challenging under varying load conditions. This study examines a ZVS tank inverter with an auxiliary LC circuit, highlighting the role of the ZVS inductor in supplying adequate reactive current during dead-time. The necessary inductance was derived theoretically and tested experimentally by changing the inductor and measuring inverter losses and spectral features. Results indicate that improper design may increase conduction and switching losses, noise, and distortion, while correct design ensures reliable ZVS. There is a trade-off: designing for the worst-case load ensures robustness but reduces efficiency at rated conditions, while optimizing for a specific load risks ZVS failure with variations. This study emphasizes the importance of designing the ZVS inductor based on actual load conditions.

Keywords: High-frequency inverter, Zero-voltage switching, Load fluctuation

I. Introduction

In recent years, demand for high-frequency inverters has increased in applications such as induction heating and wireless power transfer, driven by advances in wide-bandgap devices, such as GaN and SiC, which enable high-speed switching and the miniaturization of passive components. A key challenge is switching losses, which cause heat and potential device failure under hard switching. To mitigate this, zero-voltage switching (ZVS) is employed, where the parasitic capacitance of the switching device is charged and discharged during the dead time, allowing the drain-source voltage to reach zero before turn-on, thereby reducing losses. However, in load-resonant inverters, ZVS depends on load current, and variations in load impedance may prevent ZVS. To extend the ZVS range, a full-bridge ZVS-tank inverter [1] with an auxiliary LC circuit has been proposed. However, designing for a single operating point risks ZVS loss under load variation, while a worst-case design increases conduction and switching losses. This study experimentally investigates ZVS inductor design to minimize losses under varying load power factors.

II. ZVS tank inverter

Fig. 1 shows the ZVS-tank inverter analyzed in this paper, and Fig. 2 illustrates the general shape of the output waveforms. The circuit is configured as a full bridge, and a carrier phase shift modulation for two legs is employed. The load consists of an RLC series resonant circuit, assuming a resonant load such as a wireless power transfer system or induction heating. In this circuit, an LC circuit is connected in parallel with the lower-arm device of each leg. Hereafter, the LC circuit will be referred to as the ZVS tank. In the ZVS tank, the capacitor C_{ZVS} is designed to have half of the input voltage applied across the capacitor C_{ZVS}. When the connected device turned off, half of the DC voltage V_{in} / 2 is applied to the inductor L_{ZVS}. In contrast, when the connected device is turned on, half of the inverted DC voltage -V_{in} / 2 is applied. This voltage generates a triangular-shaped

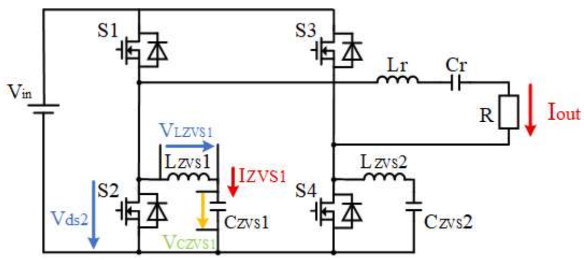

Fig.1. ZVS tank inverter.

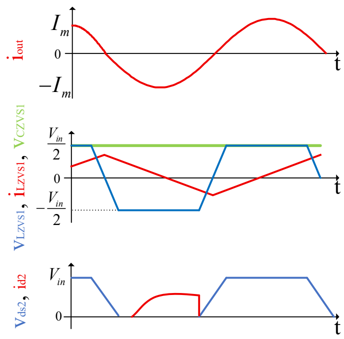

Fig. 2. Typical waveforms on ZVS-tank inverter.

reactive current from the inductor L_{ZVS}, enabling the ZVS range's expansion.

III. ZVS inductance

Fig. 3 is a schematic diagram showing how ZVS is achieved in a ZVS tank inverter. The current through the device during dead-time equals the load current I_{out} plus the ZVS tank current I_{ZVS}. The design of the ZVS inductor depends on the total charge of these currents [2].

The maximum current, which is required for ZVS tank, can be obtained from Equation (1) considering the phase shift angle and phase difference. Here, α represents the phase difference between the inverter output voltage and output current, and φ represents the phase shift angle.

$$I_{ZVS\_\max} = \frac{2Q \mp \dfrac{2I_m}{\omega}\sin\omega\left(\dfrac{t_\alpha}{2} \pm t_\phi\right)\sin\omega\dfrac{t_d}{2}}{t_d\left(1-\dfrac{t_d}{T}\right)} \quad \cdots\cdots\cdots\cdots\cdots (1)$$

Converting this to an inductance equation allows the ZVS inductor to be determined from Equation (2).
Here, $t_\alpha / 2$ represents the phase shift angle, and t_φ represents the phase difference converted to time.

$$L_{ZVS} = \frac{V}{4I_{ZVS\_\max}}\left(\frac{T}{2}-\frac{t_d}{4}\right) \quad \cdots\cdots\cdots\cdots\cdots\cdots\cdots\cdots\cdots\cdots\cdots (2)$$

IV. Experimental results

Loss measurements were conducted while varying the ZVS inductor. Table 1 shows the experimental parameters. Fig. 4 shows the experimental circuit. To confirm losses due to excessive current in L_{ZVS}, the losses generated were measured using a power meter (PW6001). Due to the limited frequency bandwidth of the power meter (PW6001), the output from the load-side LC resonant circuit was converted to DC using a diode bridge rectifier. Losses were then measured based on the input and output DC power. Under a fixed output power of 200 W, the load inductance L_r and load resistance R were varied to adjust the power factor. Measurements were performed for three load power factors: 1, 0.9, and 0.8.

Fig. 6 shows the losses when varying L_{ZVS} at different power factors. The vertical axis represents the generated loss, and the horizontal axis represents the L_{ZVS} inductance value. Results showing operation with L_{ZVS} removed from the circuit are denoted as infinite inductance. At a unity power factor, the loss is minimized at L_{ZVS} = 1 μH, which is the maximum inductance value where ZVS is achieved. Below 1 μH, the loss increases. Reducing the inductance below 1 μH leads to higher losses due to excessive current through the ZVS inductor. Furthermore, for power factors of 0.9 and 0.8, where ZVS is already achieved, the losses still reach a peak at 0.5 μH. This corresponds to the inductance value at which the current through the ZVS inductor is maximized. Losses decrease by increasing the inductance value to reduce the current through the ZVS inductor.

The results indicate that carefully selecting L_{ZVS} is essential to achieve an optimal trade-off between maintaining ZVS operation and minimizing total losses, thereby improving overall circuit efficiency.

References

[1] Ryohei Okada, Ryosuke Ota and Nobukazu Hoshi : "Novel Soft-Switching Active-Bridge Converter for Bi-directional Inductive Power Transfer System", in IEEJ Journal of Industry Applications, Vol.11, No.1, pp.97-107 (2021)

[2] Masamichi Yamaguchi, Hiroki Watanabe, Keisuke Kusaka, Jun-ichi Itoh : "Implementation Method of Inverter Circuit for Continuous Megahertz and Kilowatt Operation", in IEEJ Journal of Industry Applications, Vol.144, No.5, pp.399-499 (2023)

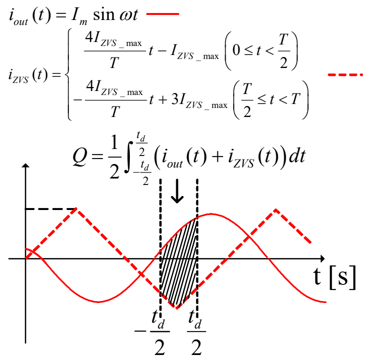

Fig. 3. Current on switching devices at ZVS operation.

Table 1. Experimental parameter

Parameters	Symbol	Value
Input voltage	V_{DC}	100V
Phase shift angle	α	0 deg
Output frequency	f	3 MHz
Dead-time	td	33ns
Resonant Inductor	L_r	20.2 uH
Resonant capacitor	C_r	141.1pF
Capacitance of Czvs	C_{ZVS1}, C_{ZVS2}	240nF
Output Power	$Pout$	200W

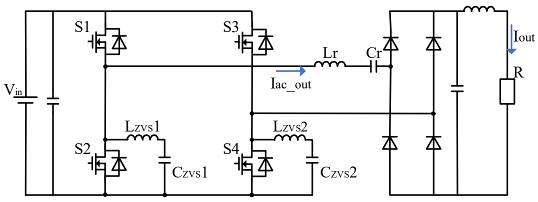

Fig. 4. Experimental circuit.

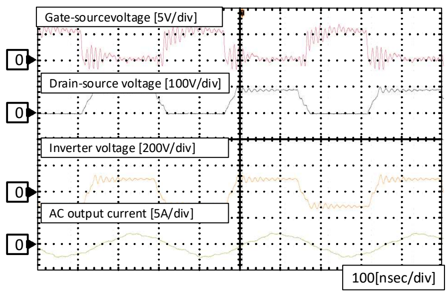

Fig. 5. Output waveform (P.F. = 0.9).

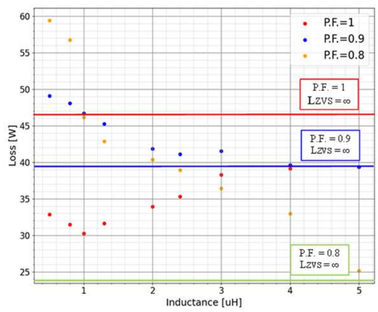

Fig. 6. Loss vs. Lzvs