Reduction of parasitic capacitance in PCB planar inductor based on geometry considerations

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Abstract The rising demand for high-efficient power systems has driven the development of wide-bandgap power devices, through which higher power density and better miniaturization could be achieved. To further improve system efficiency and reduce unwanted losses, passive components, especially passive inductors, are also required to have good high-frequency characteristics. In this paper, printed circuit board (PCB) inductor, a type of inductor known for having consistent, excellent high frequency characteristics through trace geometry design, is considered, and methods for enhancing frequency characteristic by reducing the turn-to-turn winding parasitic capacitance of PCB inductor are introduced, evaluated experimentally, and reported herein.

Key words PCB inductor, frequency characteristic, parasitic capacitance, octagonal coil, coil length, substrate capacitance

1. Introduction

The global demand for electricity is rising significantly due to the transition from fossil fuel to electricity consumption, as well as the rapid expansion of electrification in most aspects of our lives. From the visible electric vehicles to the invisible AI workloads, the increasing need for power, followed by the requirement for efficient power conversion has always been a challenging task to solve. As part of the solution process, wide-bandgap power devices (SiC, GaN) are utilized to operate power electronic circuits at higher frequency, enabling faster switching while minimizing conduction and switching losses, thereby achieving better efficiency.

The realization of a high-frequency power conversion system relies not only on the wide-bandgap power switches but also on the surrounding components – including the passive elements in the circuit. Passive components refer to inductors, capacitors, resistors, etc., and they are also required to be equally capable at high frequencies in order not to negate the whole circuit efficiency. In this paper, the primary subject of discussion is the inductor. Due to non-ideal behavior caused by parasitic components, at high frequencies,

inductors lose their inductive characteristic and behave more like capacitors, which is undesirable and problematic for circuit operation.

Printed circuit board (PCB) inductors are inductive components formed directly on PCB substrates and are usually implemented in a spiral pattern and planar shape. By integrating the inductor into the board layout, miniaturization is achieved. Compared to traditional inductors, they offer many advantages such as ease of fabrication, precise dimensional control, mechanical stability and are applicable to high-frequency applications such as RF circuits, power converters, and EMI filters. The performance of PCB inductors is strongly influenced by the board material properties, wiring geometry, coil shape, and parasitic components such as interwinding capacitance and conductor loss, which may limit the inductance, quality factor Q, and high-frequency attenuation. Therefore, in this paper, by investigating possible methods that help reduce parasitic capacitance, an improvement in the frequency characteristic is expected. Two methods considering the geometry of PCB inductor - one examining the effect of air-core size on coil length, and the other addressing the PCB substrate parasitic capacitance cancellation - are investigated

and the effectiveness in improving PCB inductor frequency characteristic is verified through experimental results.

2. Introduction of PCB inductor

In this paper, a simple planar single-layer PCB inductor with an octagonal spiral pattern is utilized to confirm the frequency characteristic and the validity of the proposed parasitic capacitance cancellation method. The inductor and its basic parameters are presented in Fig. 1 and Table 1, respectively.

Compared to regular octagonal spiral pattern, the pattern of PCB inductor in Fig. 1 is less symmetrical due to the rectangular air core in the middle of the inductor. Therefore, to model this PCB inductor, some adjustments in the calculation formula are necessary.

Firstly, to calculate the inductance, modified Wheeler formula for octagonal spiral inductor is applied, in which the average diameter of the coil $d_{avg} = 0.5 \times (d_{inner} + d_{outer})$ and the fill factor $\emptyset = (d_{outer} - d_{inner})/(d_{outer} + d_{inner})$.

$$L_s = 2.25 \times \mu_0 \times \frac{n^2 \times d_{avg}}{1 + 3.55 \times \emptyset} \tag{1}$$

Next, the series resistance is calculated while considering the skin effect. At high frequencies, the induced eddy current in the inductor trace opposes the current flow, causing the current to concentrate near the conductor's surface. This effect significantly reduces the effective cross-sectional area, and due to the inversely proportional relation, the conductor's resistance is also increased, which in this case is the series resistance of PCB inductor. The skin depth δ and the resistance are calculated using the following formulas, in which f is the frequency, h_t is the copper thickness and l is the trace length introduced later.

$$\delta = \sqrt{\frac{\rho_{Cu}}{\pi \times f \times \mu_0 \times \mu_{r_{Cu}}}} \tag{2}$$

$$R_s = \rho_{Cu} \frac{l}{w_t \times \delta \times (1 - e^{-(h_t/\delta)})}$$
 (3)

Another important parameter for modeling PCB inductor is parasitic capacitance. In a simple planar PCB inductor, the main parasitic components include turn-to-turn parasitic capacitance between traces C_p and stray capacitance from the trace through the substrate to ground C_{FR4} . In particular, as shown in Fig. 2 (a), the

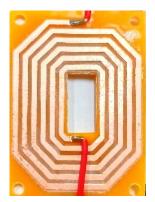


Fig. 1. Octagonal spiral PCB inductor.

Table 1. Design parameters.

Parameter	Symbol	Value	Unit
Trace width	w_t	0.0015	m
Trace spacing	S	0.001	m
Air core width	w _{air}	0.008	m
Air core height	h_{air}	0.016	m
Inner diameter (vertical)	d_{inner}	0.018	m
Outer diameter (vertical)	d_{outer}	0.046	m
Copper thickness	h_t	35×10 ⁻⁶	m
Substrate FR4 thickness	h_{FR4}	0.001565	m
PCB thickness	h_{PCB}	0.0016	m
Distance from air core to the neareast turn	а	0.001	m
Number of turns	n	5.5	
Copper resistivity	ρ_{Cu}	1.7×10 ⁻⁸	Ω m
Copper relative permeability	μ_{r_Cu}	1	
FR4 dielectric permittivity	ε_{r_FR4}	4.4	
FR4 volume resistivity	$ ho_{FR4}$	10^{13}	Ωm
Vacuum permittivity	ε_0	8.854×10 ⁻¹²	F/m
Vacuum permeability	μ_0	4π×10 ⁻⁷	H/m

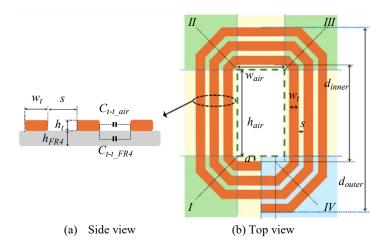


Fig. 2. PCB inductor layout.

turn-to-turn parasitic capacitance between traces C_p comprises two components: one is the turn-to-turn parasitic capacitance via a dielectric layer of air, and the other is the parasitic capacitance between traces via a dielectric layer of PCB substrate, which is FR4 material in this case. Even though most parameters are identical, the difference between the relative permittivity of air and substrate's material would create a significant difference between the two kinds of capacitance value and further increase the total parasitic value. Meanwhile, via the substrate layer, stray capacitance between traces and ground also exists, contributing to the PCB inductor's parasitic behavior. In consideration of the modeling approach, the substrate's resistance R_{FR4} will be included and placed parallel to the stray capacitance C_{FR4} . Calculations of the explained parameters are expressed as follow:

$$C_p = C_{t-t_{air}} + C_{t-t_{-FR4}}$$

$$= (1 + \varepsilon_{r_{-FR4}}) \times \varepsilon_0 \times \frac{h_t \times l}{s}$$
(4)

$$C_{FR4} = \frac{1}{2} \times \varepsilon_0 \times \varepsilon_{r_FR4} \times \frac{l \times w_t}{h_{FR4}}$$
 (5)

$$R_{FR4} = 2 \times \rho_{FR4} \times \frac{h_{FR4}}{l \times w_t} \tag{6}$$

From the above formulas, there is one parameter that is not yet determined - the trace length l. To precisely calculate and evaluate the parasitic capacitance of the PCB inductor, it is necessary to obtain the length as accurately as possible. The trace length formula for a symmetrical octagonal spiral PCB inductor is well-established in much previous research, but in the case when the coil shape is not symmetrical due to the air core size as the coil in Fig. 1, the developed equations below can be utilized to compute the exact length. Looking at Fig. 2 (b), the coil is separated into three main sections separated by the marked color. The green section with marked number I, II, III are equal and can be calculated using equation (7). The blue section indicated with number IV where the coil turns differently compared to other green sections is computed by expression (8). The remaining part of the coil is highlighted in yellow and can simply be determined by formula (9) based on the air core size. The total trace length, as defined in equation (10), is the sum of the trace lengths calculated from three green sections, one

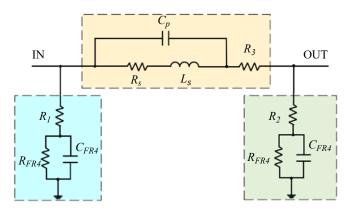


Fig. 3. π model of PCB inductor.

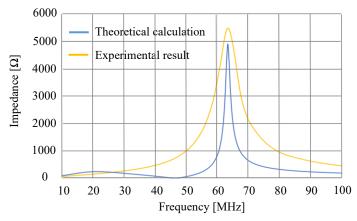


Fig. 4. Comparison between theoretical calculation and experimental result.

blue section, and one yellow section. The formula (10) is derived for an integer turn number, so if the number of turns is decimal, additional calculations using Eqs. (7), (8), (9) are applicable. Supposing all corners are 135° and the coil parameters satisfy the condition of $0.5 \times w_{air} + a \ge w_t + s$. The case which $0.5 \times w_{air} + a < w_t + s$ is not considered here as it is not practical to have a PCB inductor with such large trace width and trace spacing.

$$l_{I} = l_{II} = na\sqrt{2} + 2n(\sqrt{2} - 1)w_{t}$$

$$+ \sum_{i=1}^{n} (4i - 4)(\sqrt{2} - 1)(w_{t} + s)$$

$$l_{IV} = 0.5nw_{air} + 2na + 2n(\sqrt{2} - 1)w_{t}$$

$$+ \sum_{i=1}^{n} (4i - 3)(\sqrt{2} - 1)(w_{t} + s)$$

$$(8)$$

$$l_{yellow} = 2nh_{air} + 1.5nw_{air}$$

$$(9)$$

$$l_{total} = 3l_{I} + l_{IV} + l_{yellow} = (3\sqrt{2} + 2)na + 8n(\sqrt{2} - 1)w_{t}$$

$$+2nh_{air}+2nw_{air}+\sum_{i=1}^{n}(4i-3)(\sqrt{2}-1)(w_t+s) \qquad (10)$$

From the above calculation, a π model of PCB inductor is

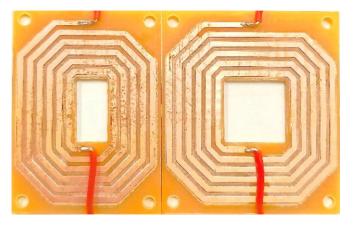
established and illustrated in Fig. 3. In addition to the components calculated above, there are three extra parameters of R_1 , R_2 , and R_3 in the model, which are expected to represent the impedance of the measurement system. Using this π model, the admittance of each branch is first calculated, then transformed into S parameters and lastly into impedance values. By substituting the input parameters in Table 1 into formulas and calculating all the necessary values for the model in Fig. 3, a frequency characteristic of the PCB inductor is obtained and demonstrated in Fig. 4. The result shows that even though the impedance value does not match with that of the experimental result, the aligned resonant frequency characteristic of PCB inductor.

3. Air core size effect on frequency characteristics

In this paper, an improvement in the PCB inductor frequency characteristic is realized by reducing the parasitic capacitance components as much as possible. From all the explained formulas above, one noticeable point is that all parasitic capacitance components are proportional to the coil length. This implies that reducing the trace length helps reduce the parasitic capacitance of PCB inductor and thereby increases the self-resonant frequency, according to Eq. (11) below. One effective method to shorten the coil length is to change the shape and size of the air core. Since the length can be minimized without affecting the inner and outer diameters of the coil, the impact on the inductance value is mitigated while the parasitic components are notably reduced. To verify the prediction, two PCB inductors with different air core sizes as seen in Fig. 5 are created and measured. By keeping the air core height the same in both cases, except for the coil length, other parameters are identical between the two inductors, including the inner and outer diameters.

$$f_{SRF} = \frac{1}{2\pi\sqrt{LC}} \tag{11}$$

With the same core height of 16mm, when the core width decreases from 16 to 8mm, the total coil length calculated using Eq. (10) decreases by 20.45%. From the measurement results in Fig. 6, the PCB inductor with air core of 16×8 mm has an inductance and



(a) Air core 16mm x 8mm

(b) Air core 16mm x 16mm

Fig. 5. PCB inductor with different air core size.

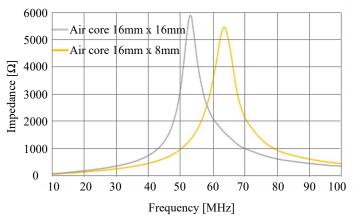


Fig. 6. Comparison of frequency characteristic between two PCB inductors with different air core size.

resonant frequency of 1.14 µH and 62.62 MHz, respectively. As for the case of square air core sized 16×16 mm, the inductance of 1.44μH and resonant frequency of 52.93 MHz are observed. Even though the outer and inner diameter are the same for both cases, the inductance still decreases. This can be explained due to the design method, the PCB inductor with the square air core has unintentionally changed its inductive behavior to be more like a PCB square pattern spiral inductor, which is outside the scope of this paper. Despite the fact that two PCB inductors have slightly different inductance value, the decrease in parasitic capacitance leading to an increase in self-resonant frequency is still notable. From the viewpoint of the PCB inductor with larger air core, with the parasitic capacitance remains unchanged, reduction in inductance value alone is not enough to improve the resonant frequency by up to 10 MHz. Therefore, the parasitic capacitance reduction method based on PCB inductor geometry by considering air core size to reduce the total

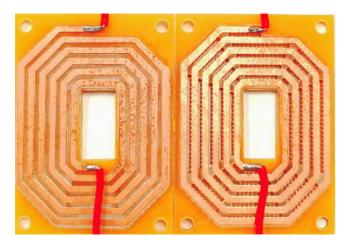
coil length is practical in improving PCB inductor resonant frequency. Moreover, the coil shape can be modified to maintain the same inductance and the validity of the method can be further proven.

4. Proposed cancellation method for PCB substrate parasitic capacitance

As mentioned above when explaining the existing parasitic capacitance in a PCB inductor, the turn-to-turn parasitic capacitance between traces, consisting of capacitances that take air and PCB substrate as dielectric layer, is significantly affected by the dielectric permittivity of the substrate. In this paper, the FR4 material of PCB substrate has a dielectric permittivity up to 4.4, which is 4 times that of air, contributes greatly to the total parasitic capacitance value. A simple yet challenging approach to reduce PCB substrate parasitic capacitance is to eliminate the substrate between traces by drilling holes through the circuit board. The idea is straightforward: if the substrate between traces were to be removed, the PCB substrate parasitic capacitance would no longer exist, which would considerably reduce the total turn-to-turn parasitic capacitance. This approach is conceptually simple because drilling hole can easily be done while fabricating the circuit board, but practically challenging due to the structural instability when all the coil turns are separated from each other and the main board.

In consideration of the effectiveness of the proposed cancellation method and the stability of PCB inductor, the first model of PCB inductor with a through hole drilled between traces is realized and demonstrated in Fig. 7. For structural firmness, at each corner of the octagonal spiral pattern, a short segment of 2-mm-long FR4 substrate is kept and the rest of the trace spacing is disposed. A comparison of the frequency characteristics between the PCB inductor with no through hole and the PCB inductor applied the proposed method is conducted, and the result is illustrated in Fig. 8.

As seen in the measurement result, the PCB inductor with through holes exhibits a slight increase in resonant frequency. Specifically, with the proposed method, resonant frequency is improved about 1.21 MHz from 62.62 to 63.83 MHz. As the inductance remains unchanged, a decrease of approximately 0.21 pF in parasitic



- (a) No through hole
- (b) With through hole

Fig. 7. Application of the proposed cancellation method on PCB inductor.

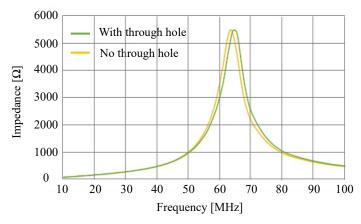


Fig. 8. Effect of the proposed cancellation method on frequency characteristic.

capacitance is confirmed. According to theoretical calculation and prediction using the π model, a complete elimination of PCB substrate between traces would decrease about 0.83 pF of parasitic capacitance; while the experimental result shows the opposite outcome with only 25.55% of the expected value is reduced. This implies that even though most of the substrate between traces is cut off, the small remaining part of FR4 still has a significant impact on parasitic capacitance. Therefore, further investigation on the relationship between the parasitic capacitance and the residual PCB substrate after applying the proposed method is necessary to realize the original design goal while maintaining good PCB inductor structural stability. Even so, this approach is promising among many methods to fully cancel the PCB substrate parasitic capacitance.

5. Conclusion

This paper focuses on improving the frequency characteristic of a single layer PCB planar inductor based on the reduction of parasitic capacitance by adopting 2 different approaches: adjusting the total coil length or eliminating PCB substrate between traces. The trace length can be minimized using a smaller air core with its height remained unchanged so as not to affect the inner and outer diameters of the coil, resulting in a decrease in parasitic capacitances while maintaining the inductance value. Meanwhile, the second method focuses on complete cancellation of the PCB substrate parasitic capacitance between traces by drilling hole in the trace spacing. The initial validation of the two methods provides promising results from which the effectiveness of the proposed approaches is verified. Even though further adjustment and investigation are required, the two proposed geometrical approaches are expected to significantly increase the frequency characteristic, enabling PCB inductor utilization in high-frequency application such as RF circuits, wireless systems, EMI noise filters, etc.

6. References

- S. S. Mohan, M. del Mar Hershenson, S. P. Boyd, and T. H. Lee, "Simple accurate expressions for planar spiral inductances," *IEEE Journal of Solid-State Circuits*, vol. 34, no. 10, pp. 1419–1424, Oct. 1999, doi:10.1109/4.792620.
- [2] M. Derkaoui, Y. Benhadda, A. Hamid, and A. Temmar, "Design and modeling of octagonal planar inductor and transformer in monolithic technology for RF systems," *Journal of Electrical Engineering & Technology*, vol. 16, no. 3, pp. 1481–1493, Mar. 2021, doi:10.1007/s42835-021-00692-x.
- [3] A. B. Islam, S. K. Islam, and F. S. Tulip, "Design and optimization of printed circuit board inductors for wireless power transfer system," *Circuits and Systems*, vol. 4, no. 2, pp. 237–244, Jan. 2013, doi:10.4236/cs.2013.42032.
- [4] A. Ammouri, H. Belloumi, T. B. Salah, and F. Kourda, "Experimental analysis of planar spiral inductors," in *Proc. 2014 International Conference on Electrical

- Sciences and Technologies in Maghreb (CISTEM)*, Tunis,
 Tunisia, pp. 1–5, 2014,
 doi:10.1109/CISTEM.2014.7076937.
- [5] S. Luan *et al*., "Design guidelines to reduce parasitic capacitance in planar inductors," in *Proc. 2023 IEEE Applied Power Electronics Conference and Exposition (APEC)*, Orlando, FL, USA, pp. 1579–1585, 2023, doi:10.1109/APEC43580.2023.10131294.
- [6] L. Wan *et al*., "Optimal design of single-layer and multi-layer air-core inductors considering uncertainty factors," *IEEE Access*, vol. 11, pp. 134460–134472, 2023, doi:10.1109/ACCESS.2023.3336572.
- [7] S. Lee, S. Kim, J. W. Shin, *et al*., "Analyzing and mitigating parasitic capacitances in planar transformers for high-frequency operation," *Journal of Power Electronics*, vol. 24, pp. 946–954, 2024, doi:10.1007/s43236-024-00804-6.
- [8] C. K. Lee, Y. P. Su, and S. Y. Ron Hui, "Printed spiral winding inductor with wide frequency bandwidth," *IEEE Transactions on Power Electronics*, vol. 26, no. 10, pp. 2936–2945, Oct. 2011, doi:10.1109/TPEL.2010.2076318.
- [9] C. K. Lee, Y. P. Su, and S. Y. R. Hui, "Printed spiral winding inductor with wide frequency bandwidth," IEEE Transactions on Power Electronics, vol. 26, no. 10, pp. 2936–2945, Oct. 2011, doi:10.1109/TPEL.2010.2076318.
- [10] H. A. Aebischer, "Inductance formula for rectangular planar spiral inductors with rectangular conductor cross section," *Advanced Electromagnetics*, vol. 9, no. 1, pp. 1–18, Feb. 2020, doi:10.7716/aem.v9i1.1346.
- [11] I. Hussain and D.-K. Woo, "Inductance calculation of single-layer planar spiral coil," *Electronics*, vol. 11, no. 5, p. 750, Feb. 2022, doi:10.3390/electronics11050750.
- [12] J. Schäfer, D. Bortis, and J. W. Kolar, "Optimal design of highly efficient and highly compact PCB winding inductors," in *Proc. 2018 IEEE 19th Workshop on Control and Modeling for Power Electronics (COMPEL)*, Padua, Italy, pp. 1–8, 2018, doi:10.1109/COMPEL.2018.8460166.