

Miniaturization of Inductor in Grid-Tied Inverter Utilizing a Wideband Four-Terminal Virtual Impedance Circuit

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Abstract—Reducing the size of inductors in grid-tied inverters is essential for increasing the power density of power conversion systems (PCSs). While increasing the switching frequency can help decrease inductor size, this approach presents challenges in high-power PCSs due to increased switching losses and device limitations. Alternatively, a two-terminal virtual impedance circuit has been proposed. However, conventional virtual impedance circuits must be connected in series with the output of PCSs, which causes the entire line current to pass through the auxiliary circuit, increasing power losses. This paper proposes a four-terminal virtual impedance circuit. The proposed virtual impedance circuit emulates a four-terminal virtual impedance network, providing electrical characteristics similar to those of passive components over a broad bandwidth. It is tested experimentally with an 800-W prototype.

Keywords—grid-tied inverter, interconnected-inductor, virtual impedance circuit, four-terminal network theory

I. INTRODUCTION

In recent years, grid-tied inverters for photovoltaic systems have been actively studied [1-2]. Alongside this trend, advancements in the processing speed of power electronic converter controllers have enabled high-performance current and voltage control [3]. To supply power from photovoltaic systems to the utility grid, a power conversion system (PCS) is required. To enhance the power density of PCS, it is essential to reduce the size of the interconnected inductor, which occupies a large portion of the PCS volume [4-5]. In small- to medium-power PCS, one strategy for inductor miniaturization is to increase the inverter's switching frequency. However, this results in higher switching power losses. Additionally, in high-power PCSs, there are constraints on raising the switching frequency [6].

As an alternative, virtual impedance circuits have been proposed, which emulate inductive or capacitive behavior using small passive components and switching circuits [7-10]. These virtual impedance circuits can be connected in series or parallel like conventional passive components. The virtual impedance circuit can be used to reduce the size of bulky

passive elements in converters. In [9-10], a virtual impedance circuit was applied to replace the DC-link filter inductor in a motor drive system. However, conventional virtual impedance circuits operate at switching frequencies of only a few kHz, which limits their control bandwidth and makes them unsuitable for grid-tied inverters operating at several tens of kHz. Additionally, conventional virtual inductors usually utilize a two-terminal configuration. In this circuit topology, substituting the interconnected inductor results in the entire line current passing through the auxiliary circuit, which increases power losses.

To overcome these issues, this paper proposes a four-terminal virtual impedance circuit that can reduce the size of the interconnected inductor. In the proposed circuit, the auxiliary circuit conducts only the minimum necessary current required to realize the virtual impedance through a four-terminal configuration, thereby reducing power loss. As a result, the switching frequency of the auxiliary circuit can be increased, allowing for a large virtual inductance to be realized over a wide frequency range. This paper presents the circuit configuration and impedance characteristics based on four-terminal network theory and a control model for power loss-compensated DC voltage control using virtual parallel resistance. Finally, the effectiveness of the proposed circuit is validated through both simulation and experimental results.

II. OVERVIEW OF POWER CONVERSION SYSTEMS WITH PASSIVE INDUCTOR AND VIRTUAL IMPEDANCE CIRCUIT

A. Power Conversion Systems

Fig. 1 illustrates the power conversion systems (PCSs), which consist of a grid-tied inverter and an interconnected inductor. The high-power grid-tied inverter has a bulky passive inductor at the output, which prevents PCSs from downsizing. Increasing the switching frequency is an effective approach to reducing the size of inductors in grid-tied inverters. However, this method poses challenges in high-power PCSs due to increased switching losses and device constraints. This paper presents an alternative method for interconnected inductor miniaturization using a virtual impedance circuit.

B. Issues of Applying Conventional Virtual Impedance Circuits to Existing PCSs

Fig. 2 shows the concept of the conventional two-terminal virtual impedance circuit. In conventional virtual inductance control approaches, an integrator is utilized to derive the control reference. The virtual inductor model is expressed as

$$Z_{vir}(s) = \frac{v(s)}{i(s)} = sL_{vir} \quad (1)$$

where s is the Laplace operator.

According to (1), by sampling the terminal voltage $v(s)$ of the virtual impedance circuit, integrating and dividing it by the command inductance L_{vir} , the command current $i_{cmd}(s)$ is obtained. Thus, the two-terminal structure theoretically achieves electrical characteristics equivalent to those of a passive inductor [8]. The virtual impedance circuit is envisioned as a direct plug-and-play replacement for passive inductors, enabling the downsizing of existing converter systems. Moreover, the command inductance value is dynamically tunable and maintains linearity over a wide range within the control bandwidth of the virtual impedance circuit.

Fig. 3 shows the grid-tied inverter utilizing the conventional two-terminal virtual impedance circuit. To enable a plug-and-play replacement of the existing passive components in PCSs operating at several tens of kilohertz, a wideband virtual impedance circuit is required. By increasing the switching frequency to expand the bandwidth of the conventional control method, the two-terminal virtual impedance circuit can substitute for the interconnected inductor in a grid-tied inverter. However, the conventional circuits must be connected in series with the output of PCSs, causing the entire line current to flow through the auxiliary circuit, which increases power losses. This makes it difficult to raise the switching frequency and thereby achieve a wide control bandwidth. Therefore, the conventional two-terminal virtual impedance circuit is not suitable for replacing bulky passive inductors in existing PCSs.

III. PROPOSED FOUR-TERMINAL VIRTUAL IMPEDANCE CIRCUIT

A. Circuit Configuration

Fig. 4 shows the proposed four-terminal virtual impedance circuit. This circuit consists of two small inductors (L_s , L_p), a DC capacitor C_{dc} , a sampling and control circuit, and an H-bridge converter. The proposed circuit, consisting of the H-bridge converter connected in parallel with the output of the PCSs, emulates a desired virtual four-terminal impedance network. Since this circuit topology significantly reduces power loss compared to conventional two-terminal structures, it enables high-frequency operation and a wide control bandwidth. Therefore, it becomes feasible to replace bulky passive inductors in existing PCSs using the proposed circuit.

B. Derivation of the Equivalent Impedance Using Four-Terminal Network Theory

Understanding the equivalent impedance circuit is essential for verifying the behavior of the proposed circuit as a virtual

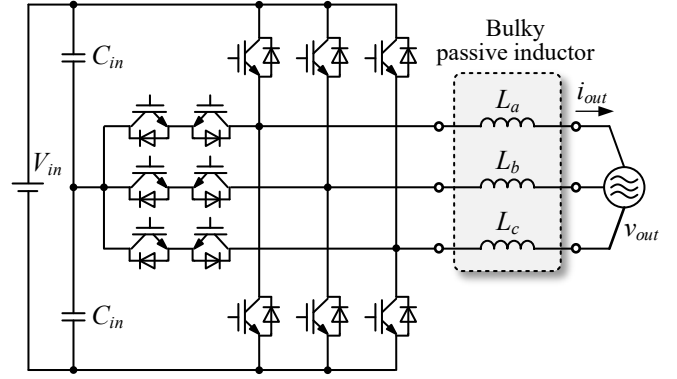


Fig. 1. A typical high-power PCS.

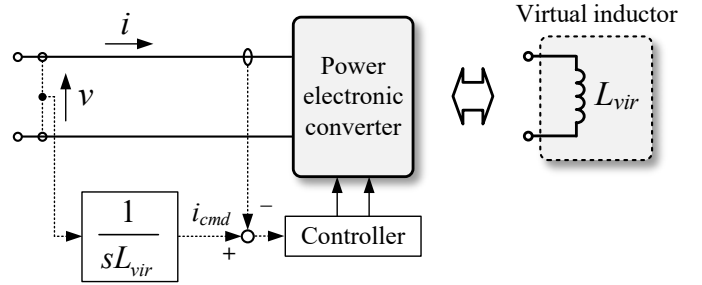


Fig. 2. Concept and equivalent impedance circuit of the conventional two-terminal virtual impedance circuit.

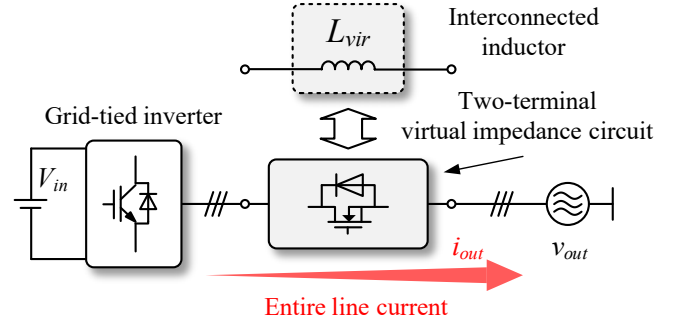


Fig. 3. Grid-tied inverter utilizing conventional two-terminal virtual impedance circuit.

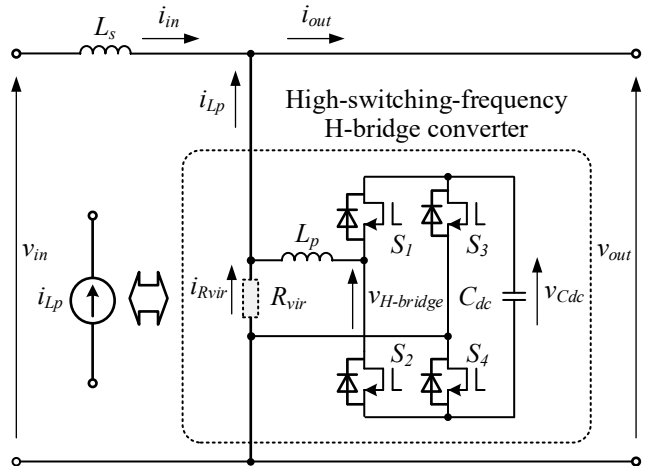


Fig. 4. Proposed four-terminal virtual impedance circuit.

four-terminal impedance network. This section presents the derivation of its equivalent impedance using four-terminal network theory.

The H-bridge converter in the proposed circuit is driven by a switching frequency much higher than that of existing PCSs, and thus behaves as a dynamically tunable current source $i_{Lp}(s)$. The proposed circuit is equivalent to a cascade connection of a small inductor L_s and a current source $i_{Lp}(s)$. Thus, the F -parameters are used in this work to derive the equivalent impedance, as they are particularly well suited for analyzing cascaded four-terminal networks. The most common definition of the F -parameters is given as follows:

$$\mathbf{F} = \begin{pmatrix} A & B \\ C & D \end{pmatrix} \quad (2)$$

$$\begin{bmatrix} v_{in}(s) \\ i_{in}(s) \end{bmatrix} = \mathbf{F} \begin{bmatrix} v_{out}(s) \\ i_{out}(s) \end{bmatrix} \Leftrightarrow \begin{cases} v_{in}(s) = Av_{out}(s) + Bi_{out}(s) \\ i_{in}(s) = Cv_{out}(s) + Di_{out}(s) \end{cases} \quad (3)$$

The F -parameters of inductor L_s and the current source $i_{Lp}(s)$ are expressed as follows:

$$\mathbf{F}_{L_s} = \begin{bmatrix} 1 & sL_s \\ 0 & 1 \end{bmatrix} \quad (4)$$

$$\mathbf{F}_{i_{Lp}} = \begin{bmatrix} 1 & 0 \\ X(s)Y(s) & Y(s) \end{bmatrix} \quad (5)$$

where $X(s)$ and $Y(s)$ are controllable parameters, and are determined by the control strategy of $i_{Lp}(s)$. According to (4-5), the F -parameters $\mathbf{F}_{total}$ of the proposed circuit are expressed as

$$\mathbf{F}_{total} = \mathbf{F}_{L_s} \mathbf{F}_{i_{Lp}} = \begin{bmatrix} 1+sX(s)Y(s)L_s & sY(s)L_s \\ X(s)Y(s) & Y(s) \end{bmatrix} \quad (6)$$

According to (3), the relationship among the input and output voltages and currents of the proposed circuit can be formally established

$$\begin{aligned} \begin{bmatrix} v_{in}(s) \\ i_{in}(s) \end{bmatrix} &= \mathbf{F}_{total} \begin{bmatrix} v_{out}(s) \\ i_{out}(s) \end{bmatrix} \\ \Leftrightarrow \begin{cases} v_{in}(s) = [1+sX(s)Y(s)L_s]v_{out}(s) + sY(s)L_s i_{out}(s) \\ i_{in}(s) = X(s)Y(s)v_{out}(s) + Y(s)i_{out}(s) \end{cases} \end{aligned} \quad (7)$$

Therefore, the equivalent impedance seen from the input two-terminal port $Z_{vir,in}(s)$, and the output two-terminal port $Z_{vir,out}(s)$ can be derived as follows:

$$Z_{vir,in} = \frac{v_{in}(s)}{i_{in}(s)} = \begin{cases} sL_s & \text{if } v_{out}(s) = 0, \\ \frac{1}{X(s)Y(s)} + sL_s & \text{if } i_{out}(s) = 0, \end{cases} \quad (8)$$

$$Z_{vir,out} = -\frac{v_{out}(s)}{i_{out}(s)} = \begin{cases} \frac{sY(s)L_s}{1+sX(s)Y(s)L_s} & \text{if } v_{in}(s) = 0, \\ \frac{1}{X(s)} & \text{if } i_{in}(s) = 0, \end{cases} \quad (9)$$

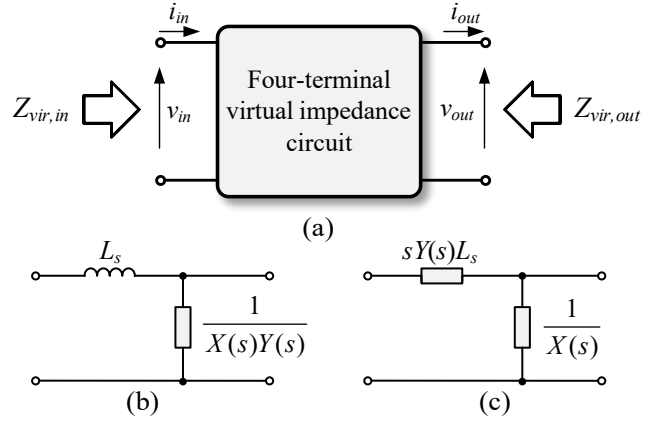


Fig. 5. Virtual four-terminal impedance network realized by the proposed circuit: (a) concept, (b) equivalent circuit as seen from the input two-terminal port, (c) equivalent circuit as seen from the output two-terminal port.

Fig. 5 shows the virtual four-terminal impedance network realized by the proposed circuit. According to (8-9) and Fig.5, the impedance characteristics realized by the proposed circuit as seen from the external ports can be concluded as follows:

- 1) If $X(s) = 0$, a passive inductor L_s is seen from the input two-terminal and cannot be tuned, whereas a virtual impedance $sY(s)L_s$ is seen from the output terminal and can be dynamically tuned by controlling $Y(s)$.
- 2) If $Y(s) = 1$, the four-terminal network seen from both the two-terminal is the L -type circuit consisting of a passive inductor L_s and virtual impedance $1/X(s)$. In particular, if $X(s) = sC_{vir}$, it becomes equivalent to an LC -filter composed of L_s and a virtual capacitor C_{vir} .
- 3) If $X(s) = sC_{vir}$ and $Y(s) = L_{vir}/L_s$, the four-terminal network seen from the output terminal becomes equivalent to an LC -filter that consists of a virtual inductor L_{vir} and a virtual capacitor C_{vir} .

The above analysis implies that the desired virtual four-terminal impedance network can be realized by appropriately adjusting the control parameters $X(s)$ and $Y(s)$.

C. Realization of the Desired Virtual Interconnected Inductor

This section describes an approach to realizing the interconnected inductor in the grid-tied inverter using the proposed four-terminal virtual impedance circuit.

The values of the control parameters $X(s)$ and $Y(s)$ are determined through the control of $i_{Lp}(s)$. Based on Kirchhoff's current law and the second row of (7), the H-bridge converter current $i_{Lp}(s)$ should be controlled according to the following expression:

$$i_{Z_{vir,Lp}}(s) = \left[\frac{1}{Y(s)} - 1 \right] i_{in}(s) - X(s)v_{out}(s) \quad (10)$$

Thus, the proposed circuit is capable of emulating the desired virtual four-terminal impedance network by regulating $i_{Lp}(s)$ based on this expression.

In order to meet grid current harmonic constraints defined by standards such as IEEE 1547 [11], the virtual four-terminal network of the proposed circuit must be equivalent to a large interconnected inductor. To realize this inductor, the control parameters $X(s)$ and $Y(s)$ are given as follows:

$$\begin{cases} X(s) = 0 \\ Y(s) = \frac{L_{vir,grid}}{L_s} \end{cases} \quad (11)$$

where $L_{vir,grid}$ is the virtual interconnected inductor realized by the proposed four-terminal virtual impedance circuit. Equation (11) indicates the basic approach for realizing a linear virtual inductor $L_{vir,grid}$, using the proposed circuit.

Based on Kirchhoff's current law and (10-11), the input currents $i_{in}(s)$ and the H-bridge current $i_{Lp}(s)$ can be expressed as follows using the output current $i_{out}(s)$

$$i_{in}(s) = \frac{L_{vir,grid}}{L_s} i_{out}(s) \quad (12)$$

$$i_{Lp}(s) = \left[1 - \frac{L_{vir,grid}}{L_s} \right] i_{out}(s) \quad (13)$$

To achieve inductor miniaturization, the proposed circuit is typically designed such that $L_{vir,grid} / L_s \gg 1$. Hence, when the proposed circuit realizes a large linear inductor $L_{vir,grid}$ over the entire control bandwidth, both the grid-tied inverter and the H-bridge converter in the proposed circuit are required to handle significantly larger currents compared to their original operation. Therefore, the increased current causes additional power losses in both converters, ultimately posing a significant limitation to achieving higher power density in PCS.

To address the aforementioned issue, this work realizes a frequency-dependent virtual inductor $L_{vir}(s)$ by adjusting the control parameter $Y(s)$ as a function of frequency. In this approach, $Y(s)$ is configured such that the virtual inductor $L_{vir}(s)$ behaves as a small inductor L_s around the grid frequency, while a much larger inductor $L_{vir,grid}$ is emulated outside that range. This design, implemented using a notch filter, reduces the current burden on both the grid-tied inverter and the proposed circuit, thereby contributing to lower power losses. The frequency-dependent virtual inductor $L_{vir}(s)$ can be expressed as follows:

$$Y(s) = \frac{L_{vir,grid} - L_s}{L_s} \frac{s^2 + d \cdot 2\zeta\omega s + \omega^2}{s^2 + 2\zeta\omega s + \omega^2} + 1 \quad (14)$$

$$L_{vir}(s) = \left[L_{vir,grid} - L_s \right] \frac{s^2 + d \cdot 2\zeta\omega s + \omega^2}{s^2 + 2\zeta\omega s + \omega^2} + L_s \quad (15)$$

where d , ζ , and ω denote the notch depth, the notch bandwidth, and the center frequency, respectively.

D. Power Loss-Compensated DC Voltage Control

The proposed circuit emulates a virtual capacitor between the output terminals and a frequency-dependent virtual inductor, and is designed to deal with only reactive power.

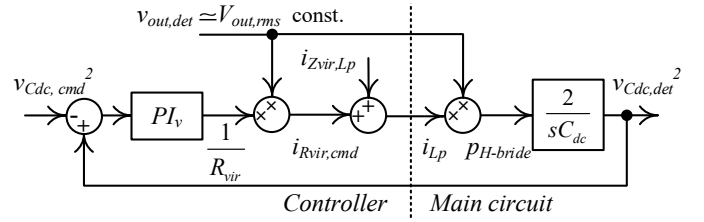


Fig. 6. Control block diagram of the linearized DC capacitor voltage control system.

Under this condition, no active power will flow into the terminal of the H-bridge converter. However, in any practical implementation, active power is discharged from the converter due to factors such as power losses [12]. This power dissipates as loss, reducing the energy stored in DC capacitor C_{dc} , leading to a drop in the DC capacitor voltage $v_{Cdc}(t)$, and consequently disrupting the proposed virtual impedance operation.

In this paper, the DC capacitor voltage control system is modeled. In order to fully compensate for power losses and regulate the voltage $v_{Cdc}(t)$, the proposed circuit is controlled to generate a virtual parallel resistance R_{vir} in Fig. 4, which models inverter loss components, including conduction losses, switching losses, and losses caused by control-induced delays. The voltage $v_{Cdc}(t)$ is obtained from the instantaneous power $p_{H-bridge}(t) = v_{out}(t)i_{Lp}(t)$ of the H-bridge converter as follows:

$$v_{Cdc}(t) = \sqrt{\frac{2}{C_{dc}} \int p_{H-bridge}(t) dt} \quad (16)$$

Note that the initial voltage of C_{dc} is assumed to be zero, and the energy of the inductor L_p is ignored. When feedback control of $v_{Cdc}(t)$ is implemented, (16) includes a square root, resulting in a nonlinear control value. This nonlinearity complicates the design and analysis of the control system. To address this, a method is adopted in which the square of the voltage is used as the control value, enabling the system to be treated as linear [13]. Fig. 6 shows the control block diagram of the linearized voltage control system using virtual parallel resistance control. The voltage control is implemented using a PI controller, and the control loop is designed such that the controller output corresponds to the reciprocal of an equivalent resistance, $1 / R_{vir}(s)$. The current $i_{Zvir,Lp}(s)$ represents the current that realizes the virtual four-terminal impedance network, and $v_{out,det}(s)$ is the output voltage of the proposed circuit. For simplicity, the output terminal voltage is assumed to be constant as $v_{out}(s) = V_{out,rms}$. The control system for the DC capacitor voltage transfer function $G_{vCdc}(s)$, is derived from Fig. 6.

$$G_{vCdc}(s) = \frac{v_{Cdc,det}^2(s)}{v_{Cdc,cmd}^2(s)} = \frac{\omega_n^2}{s^2 + 2\zeta\omega_n s + \omega_n^2} \quad (17)$$

$$\zeta = \frac{V_{out,rms} K_p}{\sqrt{2K_i C_{dc}}}, \quad \omega_n = V_{out,rms} \sqrt{\frac{2K_i}{C_{dc}}} \quad (18)$$

Where K_p is the proportional gain, K_i is the integral gain of the voltage controller PI_v .

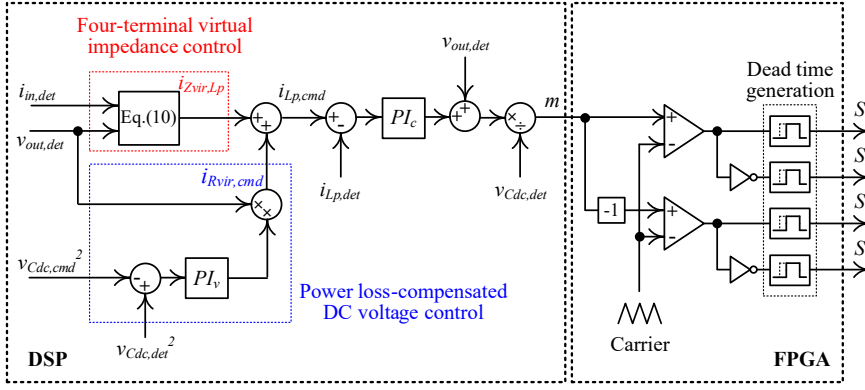


Fig. 7. Control block diagram of the proposed virtual impedance circuit.

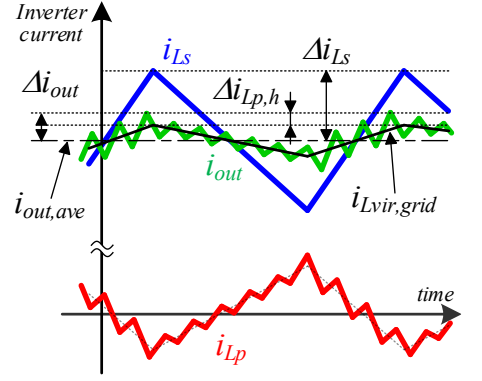


Fig. 8. The transient phenomenon of the grid-tied inverter current.

E. Control Strategies

Fig. 7 shows the control block diagram of the proposed four-terminal virtual impedance circuit. In this control, the command current $i_{Zvir,Lp}(s)$ is generated to realize the desired four-terminal impedance network, as analyzed in Section III-B and III-C. Additionally, the current $i_{Rvir}(s)$ is generated to regulate the DC capacitor voltage $v_{Cdc}(s)$ based on the analysis in Section III-D. The overall control current $i_{Lp,cmd}(s)$ is formed by summing the outputs of the four-terminal virtual impedance control path and the loss compensation control path. This signal is then used in the closed-loop inductor current control to generate the modulation index $m(s)$ for PWM regulation. The PWM signals are produced by comparing a modulation waveform to triangular carrier, generated by the FPGA, with the duty ratio command $m(s)$ provided by the DSP.

F. Estimation of Inductor Volume

In this section, the design of the inductor in the proposed circuit is described, focusing on minimizing volume. Fig. 8 illustrates the transient phenomenon of the grid-tied inverter current with the proposed virtual impedance circuit at the grid voltage peak V_m . Here, the proposed circuit is assumed to emulate the frequency-dependent virtual inductor $L_{vir}(s)$ described by (15). Note that $i_{Lvir,grid}(t)$ is the current flowing through the virtual linear inductor $L_{vir,grid}$. The output current $i_{out}(t)$ contains the high-frequency ripple component of $i_{Lp}(t)$, which is generated by the H-bridge converter. The average voltage $V_{H-bridge}$ across the output terminal voltage $v_{H-bridge}(t)$ of the H-bridge converter, taken over one carrier cycle of the grid-tied inverter, is given by the following expression.

$$V_{H-bridge} = \left[1 + \frac{L_p}{L_s} \alpha_L \right] V_m \quad (19)$$

$$\alpha_L = 1 - \frac{L_s}{L_{vir,grid}} \quad (20)$$

The inductance L_p is calculated from the high-frequency current ripple $\Delta I_{Lp,h}$ and the voltage $V_{H-bridge}$.

$$L_p = \frac{V_m L_s [V_{Cdc,ave} - V_m]}{2 f_{H-bridge} \Delta I_{Lp,h} V_{Cdc,ave} L_s - \alpha_L V_m [V_{Cdc,ave} - V_m]} \quad (21)$$

TABLE I. PARAMETERS OF THE INDUCTOR.

Parameters	$L_{vir,grid}$ and L_s	L_p
Core material	Ferrite	Powder
Core shape	E core	Toroid core
Shape factor K_V	4.8	5.5
Space factor K_U	0.4	
Saturated flux density B_{max}	0.3 T	0.7 T
Current density J	5 A/mm ²	

where $V_{Cdc,ave}$ is the average voltage of C_{dc} , and $f_{H-bridge}$ is the switching frequency of the H-bridge converter. The output current ripple requirement ΔI_{out} is regulated by the grid code. The inductance $L_{vir,grid}$ is selected such that the total output current ripple—including the high-frequency current ripple caused by $i_{Lp}(t)$ —does not exceed this limit.

$$L_{vir,grid} = \frac{V_{in} - V_m}{2 f_{inv} [\Delta I_{out} - \Delta I_{Lp,h}]} \frac{V_m}{V_{in}} \quad (22)$$

Where V_{in} , and f_{inv} denote the input voltage and the switching frequency of the grid-tied inverter, respectively. The inductance L_s is calculated from the grid-tied inverter current ripple ΔI_{in} .

$$L_s = \frac{V_{in} - V_m}{2 f_{inv} \Delta I_{in}} \frac{V_m}{V_{in}} \quad (23)$$

The inductor volume is calculated by Area Product method.

$$Vol_L = K_V \left[\frac{L_{max}^2}{K_U B_{max} J} \right]^{\frac{3}{4}} \quad (24)$$

Where K_V represents the core shape coefficient, K_U is the window utilization factor, B_{max} denotes the core's maximum flux density, and J is the current density [14]. Table I shows the parameters of the inductor. An E-core ferrite material is selected for the grid-side inductor, while a toroidal powder core is used for the inductor exposed to high-frequency currents from the H-bridge converter.

TABLE II. SIMULATION PARAMETERS FOR EVALUATION OF THE GRID-TIED INVERTER USING THE PROPOSED CIRCUITS.

Parameters of the grid-tied inverter		
Output power	P_{out}	5 kW
Input voltage	V_{in}	600 V
Output voltage	V_{out}	200 V _{rms}
Output frequency	f_{out}	50 Hz
Switching frequency	f_{inv}	10 kHz
Current ripple ratio of i_{out}	ΔI_{out}	10 %
Inductance of a virtual inductor	$L_{vir,grid}$	2.1 mH (% Z_L = 8.4 %)
Parameters of the proposed virtual impedance circuit		
Average voltage of C_{dc}	V_{Cdc}	400 V
Capacitance of C_{dc}	C_{dc}	500 μ F
Switching frequency	$f_{H-bridge}$	500 kHz
Current ripple ratio of i_{in}	ΔI_{in}	70 %
Current ripple ratio of i_{Lp}	$\Delta I_{Lp,h}$	1 %
Center frequency of a notch filter	f_{notch}	50 Hz
Cutoff frequency of PI_v	$f_{PI,v}$	10 Hz
Cutoff frequency of PI_c	$f_{PI,c}$	50 kHz

IV. SIMULATION AND EXPERIMENTAL RESULTS

A. Simulation Results

Table II shows the simulation and analysis parameters to evaluate the operation of the grid-tied inverter using the proposed four-terminal virtual impedance circuits. The virtual inductor, including the response of the current control loop $L_{vir,eff}(s)$ is expressed as follows:

$$L_{vir,eff}(s) = \frac{Y(s)L_s}{Y(s) + G_{iLp}(s)[1 - Y(s)]} \quad (25)$$

where $G_{iLp}(s)$ is the transfer function from $i_{Lp,cmd}(s)$ to $i_{Lp,der}(s)$. Fig. 9 shows the simulated frequency response of the virtual inductor $L_{vir,eff}(s)$ emulated by the proposed circuit. The influence of the notch filter is clearly observed around 50 Hz, where the response begins to dip. Outside this frequency band, the proposed circuit successfully emulates a large virtual linear inductor $L_{vir,grid}$, with the response following the ideal behavior up to approximately 50 kHz. Therefore, further extension of the current control bandwidth is essential for applying the proposed circuits to high-bandwidth applications.

Fig. 10 demonstrates the relationship between the input current ripple ratio ΔI_{in} and the inductor volume. The inductor volume is calculated, as analyzed in Section III-F. As shown in Fig. 10, the grid-tied inverter side inductors L_s in Fig. 4 occupy a majority of the total inductor volume $Vol_{L,total}$. Moreover, the volume $Vol_{L,total}$ is reduced by 60.9 % compared to the passive inductor $L_{vir,grid}$ and reaches the smallest value when the current ripple ΔI_{in} is designed at 74%.

Fig. 11(a) shows the fundamental operation waveforms of the proposed circuit under rated load conditions, based on the

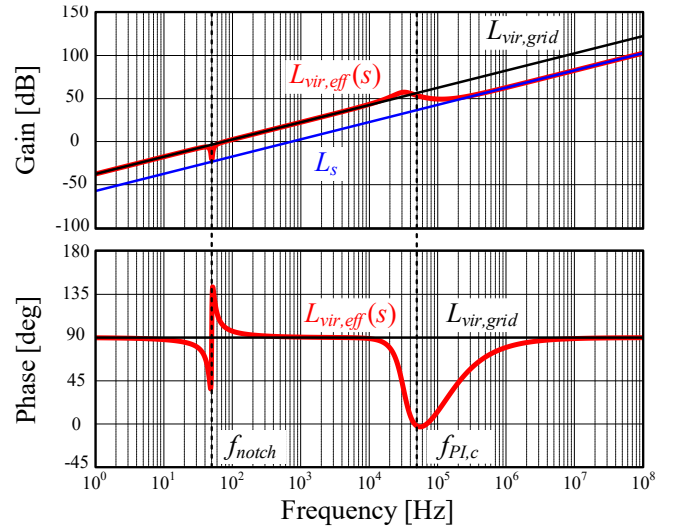


Fig. 9. Comparison of impedance characteristics between the proposed circuit and passive inductors.

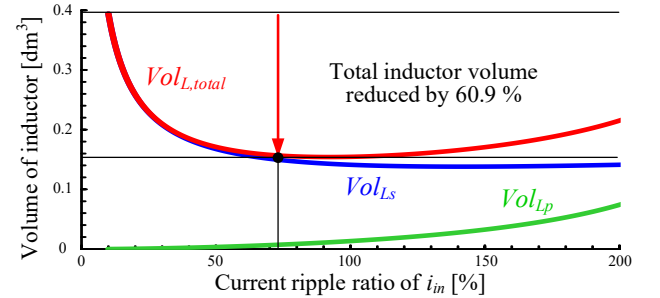


Fig. 10. Relationship between current ripple ratio of i_{in} and inductor volume.

design that minimizes the total inductor volume $Vol_{L,total}$ as shown in Fig. 10. As shown in Fig. 11(a), the DC capacitor voltage v_{Cdc} is successfully established and maintained at the desired voltage. The total harmonic distortion (THD) of the input current i_{in} which also corresponds to the output current of the grid-tied inverter, is relatively high. This is attributed to the small inverter-side inductance L_s , which reduces disturbance rejection capability and results in increased current distortion due to dead-time error voltage. On the other hand, the output current i_{out} of the proposed circuit exhibited a lower THD of 0.94%. This improvement is attributed to the proposed four-terminal virtual impedance circuit, which realizes a large virtual interconnected inductor as seen from the grid side, thereby enhancing the system's disturbance rejection capability against output voltage fluctuations.

Fig. 11(b) presents a zoomed-in view of the current waveforms. As illustrated in Fig. 11(b), the H-bridge converter current i_{Lp} is 180 degrees out of phase with the input current i_{in} , and includes high-frequency ripple harmonics. Due to the low value of L_s , the ripple current ratio of i_{in} is high, reaching up to 69.2 %. In contrast, the current ripple of i_{out} is 9.26%, as the H-bridge converter absorbs high-frequency ripple current.

These simulation results demonstrate that the proposed circuit meets harmonic standards by adjusting the impedance seen from the output terminals.

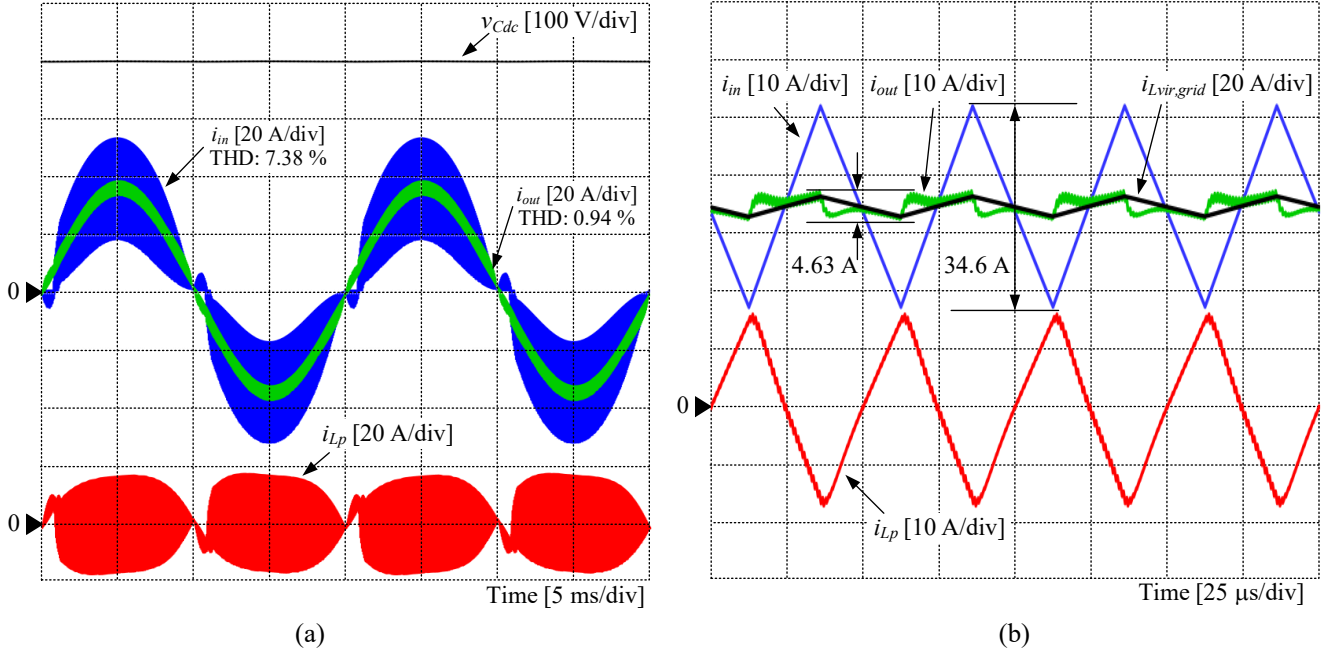


Fig. 11. Simulation results of the grid-tied inverter using the proposed circuit: (a) fundamental operation waveforms, (b) expanded view of the current waveforms shown in (a).

B. Experimental Results

To verify the basic operation of the proposed four-terminal virtual impedance circuit, an experimental test is conducted using a 2-level single-phase grid-tied inverter rated at 800 W. Fig. 12 illustrates the circuit architecture of the experimental setup. Table III presents the experimental parameters. The bulky passive inductor $L_{vir,grid}$ is replaced by the proposed virtual impedance circuit with GaN-FETs (Model: GAN080-650EBE). The virtual impedance circuit is controlled by a DSP (Model: TMS320F283790) and an FPGA (Model: SPARTAN-7). This experiment focuses on evaluating the feasibility of implementing the virtual inductor, particularly its effectiveness in suppressing disturbances caused by dead-time error voltages in the grid-tied inverter. For simplification, the grid-tied inverter is operated in open-loop control, and an RL load is used. Additionally, a DC power supply is utilized instead of the capacitor C_{dc} as in the proposed circuit.

Fig. 13 shows the experimental results of the grid-tied inverter using the proposed virtual impedance circuit. Fig. 13 (a) shows the fundamental operation waveforms. The input current i_{in} exhibits a high THD due to the decreased performance of disturbance suppression caused by the small inductance L_s . On the other hand, the output current achieves a lower THD, as the large inductance seen from the output terminals enhances the system's ability to suppress disturbances.

Fig. 13(b) presents an expanded view of the current waveforms. The ripple ratio of i_{in} reaches 74.9% due to the small inductance L_s . In contrast, i_{out} shows a reduced ripple ratio of 19.9%, as the H-bridge converter conducts only high-frequency ripple current and emulates a large inductance from the output terminals. As shown in Fig. 13, the current waveforms are similar to those in Fig. 11, confirming the operation of the proposed four-terminal virtual circuit.

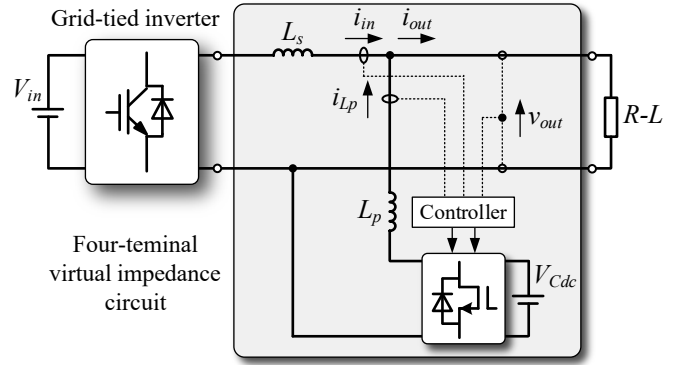


Fig. 12. Grid-tied inverter using the proposed circuit.

TABLE III. EXPERIMENTAL PARAMETERS.

Parameters of the grid-tied inverter		
Output power	P_{out}	800 W
Input voltage	V_{in}	380 V
Output voltage	V_{out}	200 V _{rms}
Output frequency	f_{out}	50 Hz
Switching frequency	f_{inv}	5 kHz
Current ripple ratio of i_{out}	ΔI_{out}	20 %
Inductance of a virtual inductor	$L_{vir,grid}$	12 mH (% $Z_L = 7.5$ %)
Parameters of the proposed virtual impedance circuit		
Average voltage of C_{dc}	V_{Cdc}	380 V
Switching frequency	$f_{H-bridge}$	150 kHz
Inductance of L_s	L_s	3 mH (% $Z_L = 1.8$ %)
Inductance of L_p	L_p	500 μ H (% $Z_L = 0.3$ %)
Cutoff frequency of PI_c	$f_{PI,c}$	15 kHz

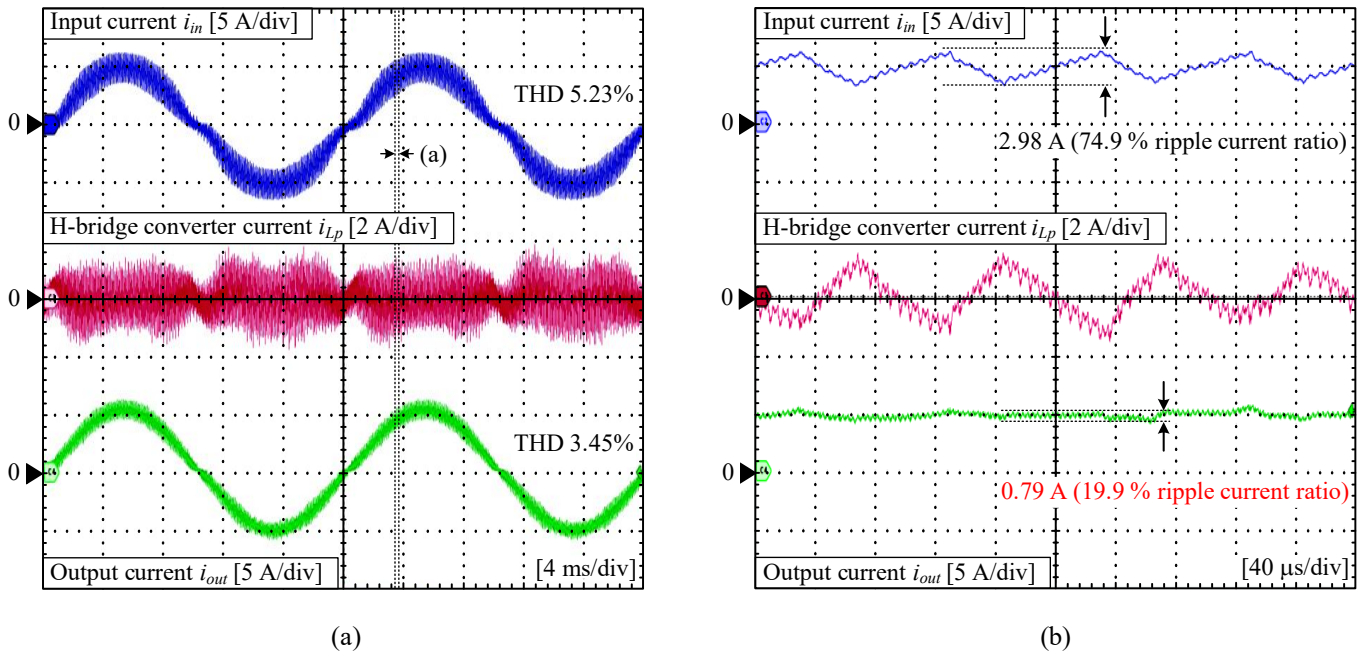


Fig. 13. Experimental results of the grid-tied inverter using the proposed circuit: (a) fundamental operation waveforms, (b) expanded view of the current waveforms shown in (a).

V. CONCLUSION

This paper presented a four-terminal virtual impedance circuit that enables the miniaturization of the interconnected inductor in grid-tied inverters. Unlike conventional two-terminal virtual impedance circuits, the proposed topology allows only the minimum required current to flow through the auxiliary circuit, thereby reducing power loss and enabling wide-band impedance emulation at high switching frequencies. The impedance characteristics were derived based on four-terminal network theory and validated through both simulation and an 800-W experimental prototype. The results demonstrated that the proposed circuit successfully emulates a large inductor while reducing the total inductor volume by 60.9% compared to a conventional passive inductor. Future work includes a detailed evaluation of power loss and thermal characteristics further to validate the circuit's feasibility for high-power applications.

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