Unbalanced Three-phase Flying-capacitor Converter for Current Ripple Reduction

Keisuke Kusaka
Dept. of Electrical, Electronics and Information Engineering
Nagaoka University of Technology
Nagaoka, Niigata, Japan
kusaka@vos.nagaokaut.ac.jp

Shinjiro Shimura
Dept. of Electrical, Electronics and Information Engineering
Nagaoka University of Technology
Nagaoka, Niigata, Japan
s235025@stn.nagaokaut.ac.jp

***Abstract*—This paper proposes a changing method for the ratio of a flying-capacitor voltage in a three-phase flying-capacitor converter (FCC), which increases output voltage levels without modifying the circuit configuration of the three-level FCC. A space vector modulation (SVM) scheme provides the degree of freedom to control the flying capacitor voltage, reducing the harmonic components of the output voltage and current at the switching frequency. Experiments with a 7-kW prototype confirm the output current ripple reduction based on the proposed SVM scheme. The reduction of the switching ripple components were confirmed from the FFT analysis results of the waveforms, and the sideband waves of the switching ripple components were reduced by 18% compared to the conventional SVM scheme. Besides, the power losses of the switching devices were analyzed to evaluate the power losses distribution. The results show that the unbalanced FC voltage does not significantly affect the device's thermal state.**

Keywords—Flying capacitor, Space vector modulation, device loss

I. INTRODUCTION

Multilevel converters have been applied in motor drive systems to meet the demand for higher power density [1]. These converters reduce harmonic components of output current and achieve higher breakdown voltage by increasing the number of output voltage levels compared to two-level inverters. The topologies of multilevel converters include neutral point clamped (NPC), cascaded H-bridge, flying-capacitor (FC), T-type, and modular multilevel converter (MMC) [2-6]. The flying-capacitor converter (FCC) topology provides advantages over others in terms of high power density, as it does not require additional DC supply or clamping diodes.

In recent years, various methods have been proposed to maintain balanced FC voltage in multilevel FCC. Among them, the carrier phase shift pulse width modulation (CS-PWM) scheme is widely used due to its simplicity as FC voltage is naturally balanced in the ideal FCC. However, an additional control loop is sometimes required due to FC voltage imbalance caused by factors such as individual device differences in the circuit when applying the CS-PWM method [7]. Moreover, it is not an optimal scheme for output current ripple reduction [8]. On the other hand, the space vector modulation (SVM) scheme allows flexible and effective use of switching states [9]. The SVM scheme in multilevel FCC reduces output voltage harmonics and maintains the FC voltage balance at the same time [10].

This paper proposes an SVM scheme for changing the ratio of FC voltage to achieve further output current ripple reduction. This SVM scheme increases the voltage levels from three to four without modifying the circuit configuration of the three-level FCC, and the FC voltage is not limited to 1/2 or 1/3 of the DC voltage. As a result, a space vector diagram with increased the number of voltage vectors is represented, through which, a better reduction in output current ripple compared to the conventional method can be realized. The proposed SVM scheme does not balance the FC voltage at 50% of DC voltage as usual. Instead, three closest voltage vectors that manage the FC voltage will be selected, resulting in the desired current ripple suppression. The proposed SVM scheme was investigated and verified through experiments with a 7-kW prototype. The losses of switching devices in the converter due to changing the ratio of FC voltage is analyzed, and evaluated for differences in losses that occur in the devices.

II. BASIC OF THREE-LEVEL FCC

A. Three-level FCC topology

The circuit configuration in Fig. 1 is the three-level, three-phase FCC. Each leg consists of four switching devices (S_{x1}, S_{x2}, S_{x3}, S_{x4}) and one flying capacitor C_x (C_u, C_v, C_w). S_{x1} and S_{x4}, S_{x2} and S_{x3} in a leg operate complementary to each other. Three-level FCC maintains the FC voltage at 50% of the DC

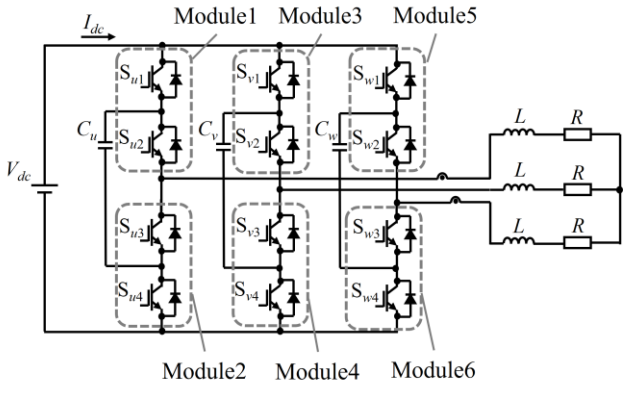

Fig. 1. Three-phase, three-level FCC topology.

voltage to achieve three-level. The output voltage is generated by the combination of the DC voltage V_{dc} and the FC voltage V_{fc}, which results in a staircase waveform due to the difference between the two voltage values. The three-level FCC in Fig. 1 allows three-level output with V_{dc} and V_{fc}.

Table 1 shows the relationship between switching states and output voltage for one phase of the three-phase three-level FCC. When FC voltage is balanced at 50% of DC voltage, switching states 1 and 2 output the same voltage. Fig. 2 shows the circuit operation modes: (a) both upper switches (S_{x1} and S_{x2}) are turned off, producing zero-phase voltage; (b) and (c) show one of the upper switches turned on, resulting in a phase voltage of $V_{dc}/2$; (d) both upper switches are turned on, resulting in a phase voltage of V_{dc}.

B. Capacitor Voltage Balancing

The balancing of the FC voltage is most important to maintain the three-level output voltage with low harmonics. The carrier phase shift modulation (CS-PWM) and space vector modulation (SVM) schemes are widely known as modulation methods for maintaining balanced FC voltage.

Fig. 3 shows the u-phase modulation wave and carrier waves of the CS-PWM scheme applied to the three-level FCC. In the CS-PWM scheme for the FCC, (n – 1) carrier waves are required to output n-level voltage. Thus, two carrier waves (C1 and C2) are used in three-level FCC, which compared with the modulation wave (M) to generate switching pulses. The generated switching pulses equalize the FC charge and discharge times and maintain a constant FC voltage. As a result, the CS-PWM scheme has features of self-balancing. However, this modulation scheme leads to poor voltage balancing by differences in device characteristics and impedance in the circuit. Thus, an additional control loop is needed, as discussed in [7].

Another modulation scheme to balance the FC voltage is the SVM scheme. In this modulation scheme of three-level FCC, 64 switching states are described as voltage vectors on the α–β coordinate in Fig. 4. Fig. 4 shows a space vector diagram consisting of 6 sectors and 24 triangles formed by 64 voltage vectors. The voltage reference $\boldsymbol{V_{ref}}$ in Fig. 4 is on the by α–β coordinate by the v_α^* and v_β^*.

$$\boldsymbol{V_{ref}} = (v_\alpha^*, v_\beta^*) \quad \cdots\cdots\cdots\cdots (1)$$

TABLE I. SWITCHING STATE AND PHASE VOLTAGE

State	$S(S_{x1}, S_{x2}, S_{x3}, S_{x4})$	V_x
0	S(0, 0, 1, 1)	0
1 2	S(0, 1, 0, 1) S(1, 0, 1, 0)	$V_{dc}/2$
3	S(1, 1, 0, 0)	V_{dc}

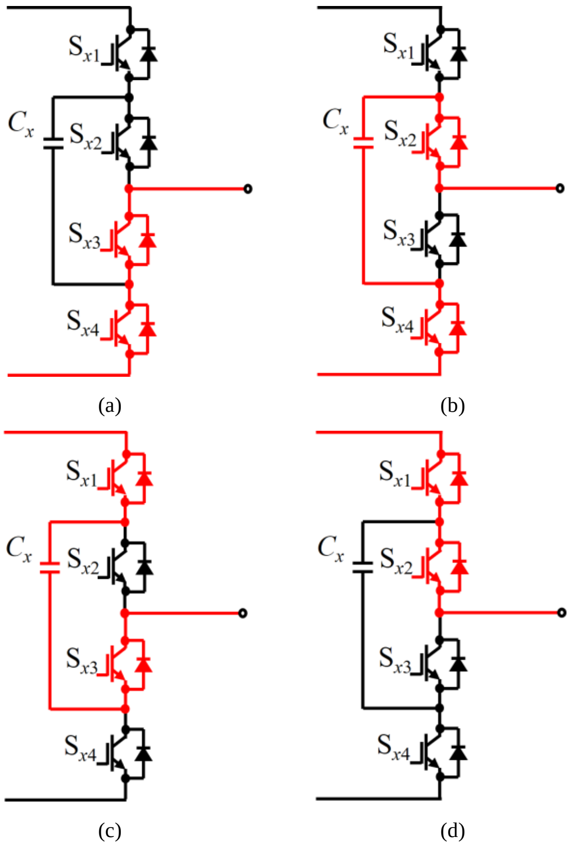

Fig. 2. Operation modes of three-level FCC. (a) state 0, (b) State 1, (c) state2, (d) State 3.

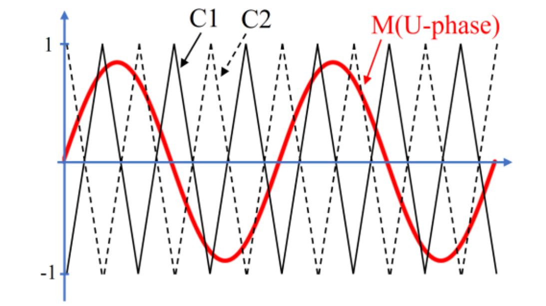

Fig. 3. U-phase voltage reference and carrier waveform applying CS-PWM of three-level FCC.

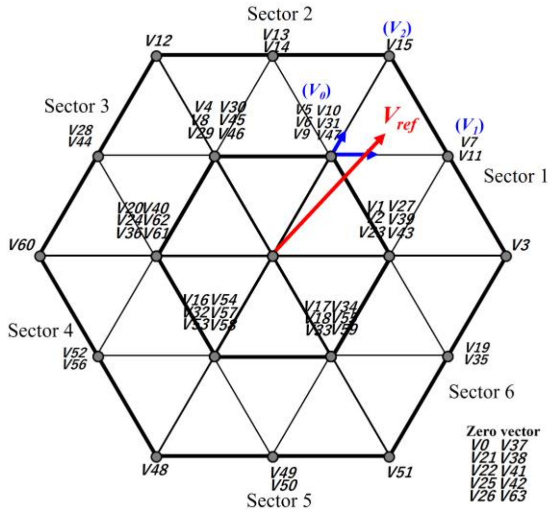

Fig. 4. Space vector diagram of three-level FCC.

$\boldsymbol{V_{ref}}$ is on one of the 24 triangles in Fig. 4. $\boldsymbol{V_0}$, $\boldsymbol{V_1}$ and $\boldsymbol{V_2}$ on triangle with $\boldsymbol{V_{ref}}$ are selected, and the duty ratio is calculated. The expressions for calculating the duty ratio of these voltage vectors are not given in this paper for brevity. $\boldsymbol{V_0}$ has six voltage vectors and $\boldsymbol{V_1}$ has two voltage vectors. These are called redundant vectors, and the optimal voltage vectors must be selected by defining a cost function for the purpose. In [9], the method was proposed to reduce the computational cost of the SVM scheme. In [11], the SVM method was proposed to reduce the voltage ripple of FC in terms of improving the FC lifespan.

III. Unbalance Operation of FC voltage

This section describes the proposed SVM scheme for changing the FC voltage ratio. The FC voltage ratio is freely changeable during operation by using this modulation scheme. For example, Fig. 5 shows the space vector diagram when the FC voltage is managed at 40% of the DC voltage. Voltage vectors are placed on the four hexagons and origin. It means that the voltage vectors do not form equilateral triangles, which differs from the balanced space vector diagram. This placement of vectors makes a relationship between the switching state and output voltage, as shown in Table 2, which allows for an increase in output voltage level. However, the conventional SVM scheme does not keep the FC voltage at desired value because of the decrease in the number of redundant voltage vectors. In this proposed SVM scheme, the optimal voltage vectors selection is performed to achieve the following two indices.

1) Maintaining FC voltage at desired value.
2) Minimizing output voltage and current ripple.

Three voltage vectors are selected to achieve the above two indices, and the duty ratios T_0, T_1, and T_2 of each vector are calculated to achieve $\boldsymbol{V_{ref}}$.

The FC charge/discharge reference Q_{fc}^{x} is calculated, which is the result of comparing the FC voltage feedback v_{fc}^{x} with the FC voltage reference v_{fc}^{*}, in order to maintain the FC voltage at desired value. Q_x^* is calculated by the following equation:

$$Q_x^* = \begin{cases} 1 & \text{if } v_{fc}^x < v_{fc}^* \\ 0 & \text{if } v_{fc}^x = v_{fc}^* \\ -1 & \text{if } v_{fc}^* < v_{fc}^x \end{cases} \text{ for } x \in \{u, v, w\} \quad \cdots\cdots\cdots (2).$$

Q_x is calculated from the switching states and polarity of the x-phase output current i_x.

$$Q_x = \begin{cases} \text{sign}(i_x) & \text{if } (S_{x1}, S_{x2}) = (\text{OFF}, \text{ON}) \\ \text{sign}(i_x) & \text{if } (S_{x1}, S_{x2}) = (\text{ON}, \text{OFF}) \\ 0 & \text{other switching states} \end{cases} \quad \cdots\cdots (3)$$

The voltage vectors are extracted where Q_x^* and Q_x are equal in the FC of the most chargeable and dischargeable phase in Fig. 5. The background colors in Fig. 5 show the regions of maximum absolute phase current at load power factor 1; -30° to 30° and 150° to 210° are most chargeable and dischargeable for U-phase FC, 30° to 90° and 210° to 270° for V-phase FC, and 90° to 150° and 270° to 330° for W-phase FC.

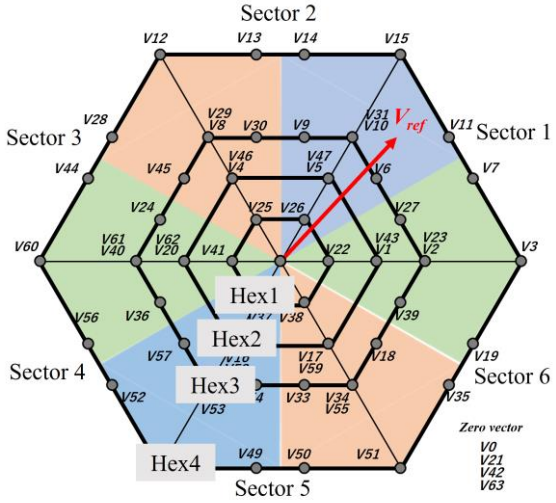

Fig. 5. Space vector diagram when FC voltage is unbalanced at 40% of DC voltage.

TABLE II. Switching State and Phase Voltage at 40% FC Voltage

State	S(S_{x1}, S_{x2}, S_{x3}, S_{x4})	V_x
0	S(0, 0, 1, 1)	0
1	S(0, 1, 0, 1)	0.4*V_{dc}
2	S(1, 0, 1, 0)	0.6*V_{dc}
3	S(1, 1, 0, 0)	V_{dc}

After that, the three vectors $\boldsymbol{V_0}$, $\boldsymbol{V_1}$ and $\boldsymbol{V_2}$ are selected from the extracted voltage vectors that satisfy the following equation.

$$l_0 = \sqrt{(v_{0\alpha} - v_\alpha^*)^2 + (v_{0\beta} - v_\beta^*)^2} \quad \cdots\cdots\cdots (3)$$

$$l_1 = \sqrt{(v_{1\alpha} - v_\alpha^*)^2 + (v_{1\beta} - v_\beta^*)^2} \quad \cdots\cdots\cdots (4)$$

$$l_2 = \sqrt{(v_{2\alpha} - v_\alpha^*)^2 + (v_{2\beta} - v_\beta^*)^2} \quad \cdots\cdots\cdots (5)$$

$$L = l_0 + l_1 + l_2 \quad \cdots\cdots\cdots (6)$$

where $v_{0\alpha}$ and $v_{0\beta}$ are the coordinates of vector $\boldsymbol{V_0}$, $v_{1\alpha}$ and $v_{1\beta}$ are the coordinates of vector $\boldsymbol{V_1}$, $v_{2\alpha}$ and $v_{2\beta}$ are the coordinates of vector $\boldsymbol{V_2}$, and $v_{\alpha*}$ and $v_{\beta*}$ are the coordinates of the voltage reference.

IV. Experimental Results

The proposed unbalanced SVM is compared among the conventional CS-PWM and balanced SVM with the experimental setup, as shown in Fig. 1. Table 3 shows the parameters used in the experiments. When the unbalanced SVM method is applied, the FC voltage is managed at 40% of

the DC voltage, and the number of levels of line voltage increases, as shown in Fig. 6. When the CS-PWM method is applied, the line voltage shows the largest switching ripple component of the line voltage.

Fig. 7 shows the FFT analysis of the line voltage for each modulation scheme. As can be seen, the harmonics of the output voltage are centered on the switching frequency, i.e., 10 kHz. The harmonics amplitude of the switching frequency component is large when using the CS-PWM scheme, but it is reduced with the SVM method. Additionally, unbalancing the FC voltage reduces the harmonics sidebands by 18 points.

Fig. 8 shows the experimental results when the FC voltage is managed unbalanced and the output frequency is 250 Hz. The FC voltage is managed to unbalance at the desired value, and the output line voltage and current are regulated at 250 Hz well.

TABLE III.

TABLE III. PARAMETERS OF EXPERIMENTAL

System parameter	Value
Switching devices	IGBT 2MBI 50N-060
DC source voltage (V_{dc})	300 V
Capacitor of DC bus (C_{dc})	4.7 mF
Flying capacitor	1.8 mF
Switching Freq. (f_{sw})	10 kHz
Output Freq. (f_{out})	50 Hz
Load resistance R	5.5 Ω
Load inductanceL	346 μH

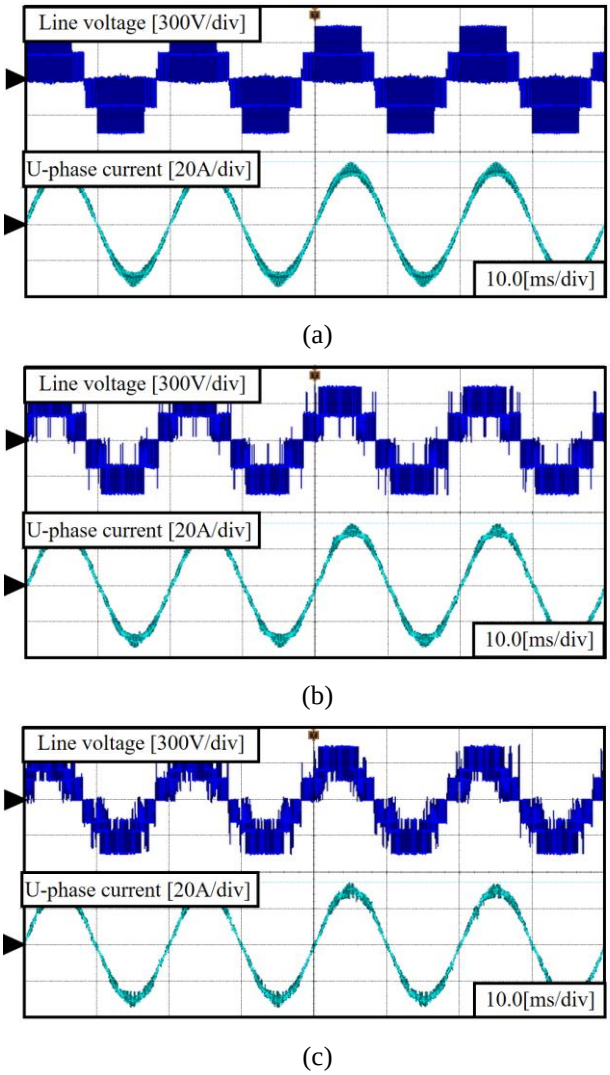

Fig. 6. Experimental results of three modulation method. (a) CS-PWM

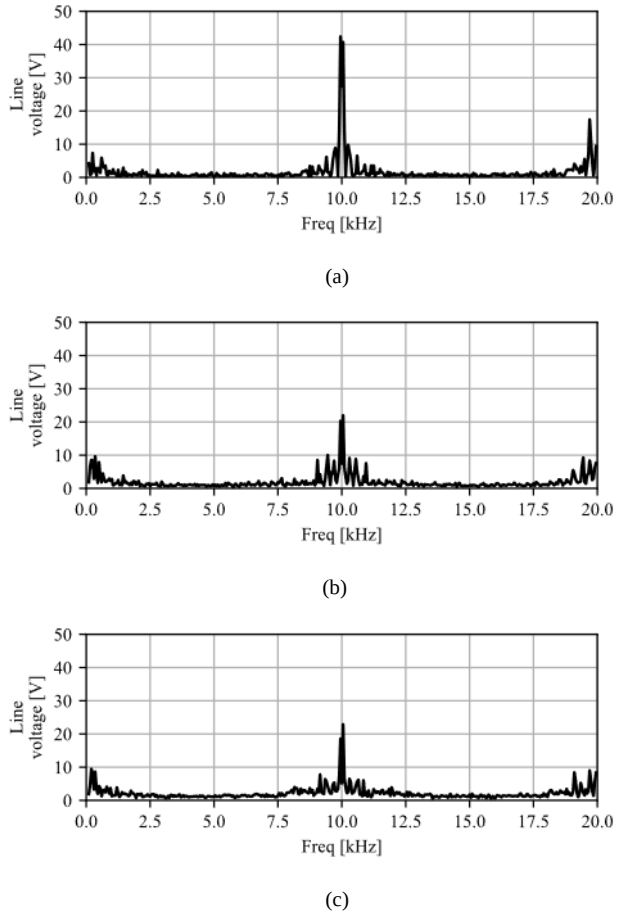

Fig. 7. FFT analysis results with three modulation schemes. (a) CS-PWM scheme. (b) Balanced SVM scheme. (c) Unbalanced SVM scheme.

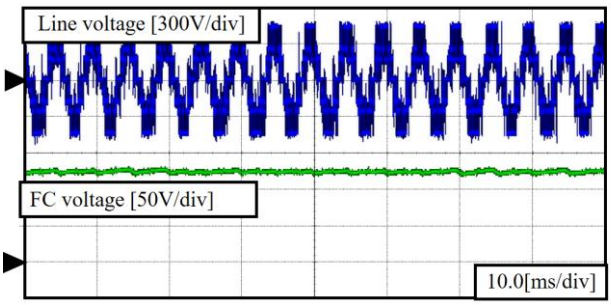

Fig. 8. Experimental results at f_{out} = 250 Hz.

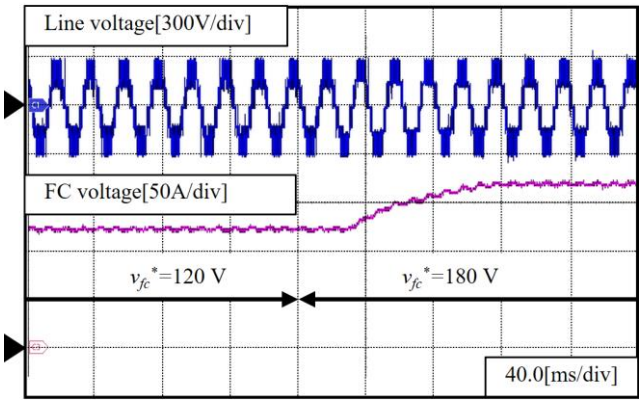

Fig. 9. The Experimental results when the FC voltage ratio is changed from 40% to 60% of DC voltage.

Fig. 9 shows the experimental results when the ratio of FC voltage is changed from 40% to 60% of the DC voltage during operation. The FC voltage is managed unbalanced at the desired value, increasing the number of output voltage levels.

V. Loss Analysis

A. Device Losses

Changing the ratio of the FC voltage may cause a thermal imbalance in the switching devices of the converter. For example, if the FC voltage is managed unbalanced using the proposed SVM scheme, the device voltage of S_{x1} and S_{x2} are different in Fig. 10. The switching losses of each device are expressed by the following equation.

$$P_{loss1} = \int_0^{T_{sw}} v_{ce1} i_c \, dt = \int_0^{T_{sw}} (V_{dc} - V_{fc}) i_c \, dt \quad \cdots\cdots (7)$$

$$P_{loss2} = \int_0^{T_{sw}} v_{ce2} i_c \, dt = \int_0^{T_{sw}} V_{fc} \, i_c \, dt \quad \cdots\cdots\cdots\cdots (8)$$

where P_{loss1}, P_{loss2} are the switching losses of S_{x1} and S_{x2}, T_{sw} is the switching frequency, v_{ce1}, v_{ec2} is the collector emitter voltage of S_{x1} and S_{x2}, i_c is the collector current. The switching losses are different by FC voltage value, and the red area in Fig. 10 shows the difference in losses between S_{x1} and S_{x2}. Thermal imbalance among switching devices decreases the converter's lifespan and lowers its efficiency. In chapter 5, the switching losses of the devices in the three-phase FCC with the proposed SVM scheme that manages unbalanced FC voltage are analyzed in detail.

B. Analysis of Device Losses

The losses of the switching device are analyzed for three modulation schemes using the circuit simulator (PLECS) with parameters in Table 3. The analysis assumed the use of two two-in-one modules per phase in Fig. 1.

Fig. 11 shows the loss analysis results for each modulation scheme in the circuit. The losses are almost unvarying for each module by all modulation schemes.

Fig. 12 shows a comparison of the losses of the four devices in the regs. There is no variation in losses for either

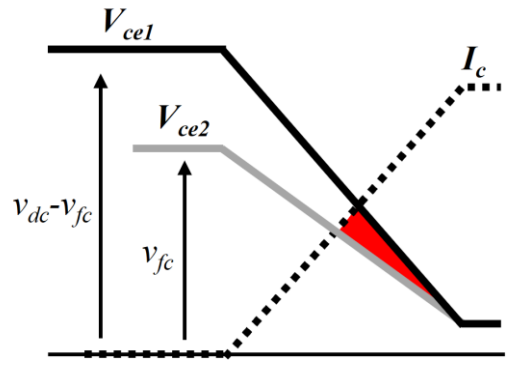

Fig. 10. Device voltage and output current when FC voltage is maintained unbalanced.

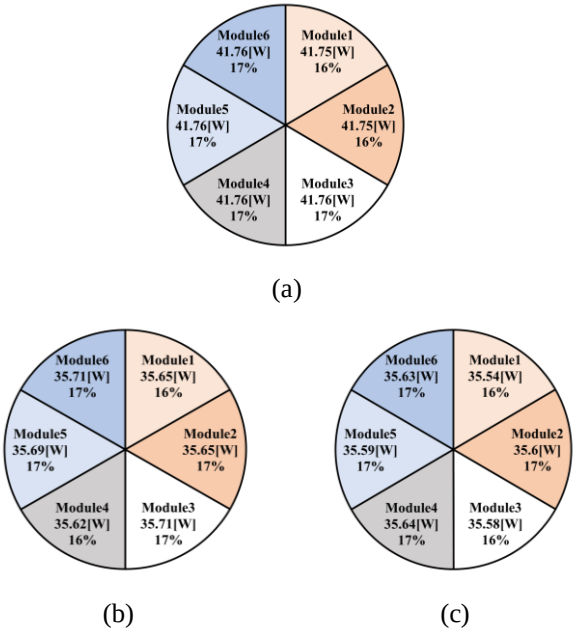

Fig. 11. Loss and percentage by modules for each modulation scheme. (a) CS-PWM scheme. (b) Balancing SVM scheme. (c) Unbalancing SVM scheme.

IGBTs and diodes when using the CS-PWM scheme or the balanced SVM scheme. However, the proposed SVM scheme resulted in device loss variation of up to 0.6 W, primarily due to the switching losses of the IGBTs. The variations in diode conduction loss and IGBT conduction loss are minimal and tend to cancel each other out, so they do not significantly affect the total device losses. As a result, the total device loss variation due to change in the FC voltage ratio remains under 1 W (approximately 0.2% of total losses) and does not significantly contribute to the heat generated by the device, as demonstrated by this analysis.

VI. Conclusion

This paper proposes an SVM scheme for changing the ratio of FC voltage to achieve output voltage and current ripple reduction. The SVM scheme increases the voltage level from three to four without changing the circuit configuration of the three-level FCC, and the FC voltage is freely determined within a defined range based on the FC charge/discharge

reference. Voltage and current ripple is reduced by selecting the three closest vectors that manage the FC voltage. Experiments conducted on a 7-kW prototype validated the effectiveness of the proposed SVM scheme, as FFT analysis showed a significant reduction in the harmonics of the switching components. Additionally, loss analysis showed minimal variation in switching device losses due to changes in the FC voltage ratio. It means that thermal imbalance does not occur even when the proposed modulation is employed. This makes the proposed SVM scheme highly useful for improving converter efficiency and reliability without increasing hardware complexity.

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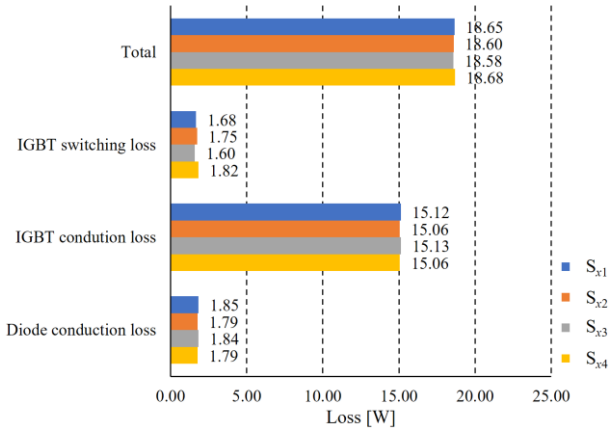

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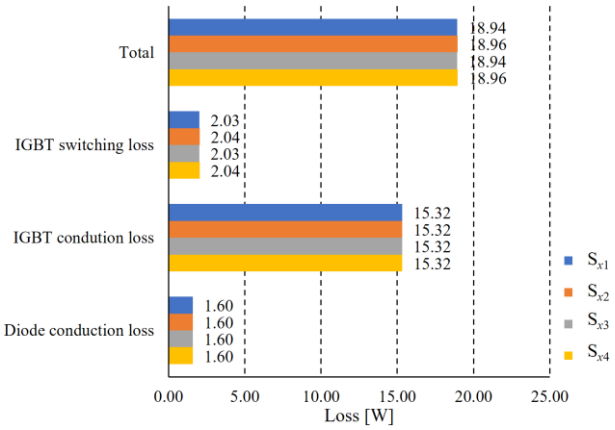

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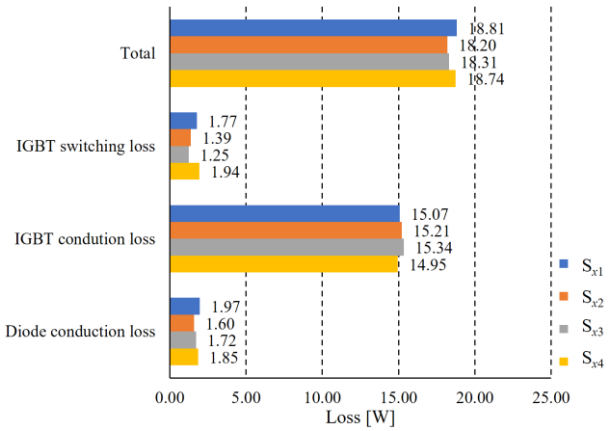

(c)

Fig. 12. Loss and percentage by modules for each modulation method. (a) CS-PWM scheme. (b) Balancing SVM scheme. (c) Unbalancing at 40% of DC voltage.