New Space Vector Modulation to Maintain Unbalanced Flying Capacitor Voltage for Output Current Ripple Reduction

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***Abstract*— This paper proposes a novel space vector modulation (SVM) strategy designed to maintaining the unbalanced flying capacitor (FC) voltage of a three-level flying capacitor converter to reduce the output current ripple. The proposed SVM strategy maintains the FC voltage unbalanced, i.e., at a voltage other than half the DC voltage. The output voltage levels are increased from three to four by unbalancing the FC voltage without changing the circuit topology. The increased number of voltage levels helps to reduce the output voltage and current ripple. However, the reduced number of redundant voltage vectors makes it difficult to maintain the unbalanced. The proposed method not only achieves a continuous ripple reduction but also keeps the unbalanced FC voltage. The proposed method is evaluated through simulation and an experiment with a 7-kW prototype. The proposed modulation reduced the current harmonics of the switching frequency by 26% and increased the converter efficiency by 0.7 points.**

Keywords—Flying capacitor, Multilevel inverter, Space Vector Modulation

I. INTRODUCTION

Nowadays, there is increasing demand for high efficiency and miniaturization of large-capacity power converters as electric vehicles and industrial equipment progress rapidly [1]. In response to this industrial requirement, multilevel converters have been widely used in recent years. They have attractive features such as high efficiency and low distortion in voltages and currents [2].

Multilevel converters reduce the harmonic components of voltage and current by increasing the number of levels in the output voltage [3–4]. Thus, a high power density of power converters becomes achievable due to the effective suppression of output harmonics without filters [5]. Over the past few decades, many different circuit topologies have been proposed as multilevel converters [6], such as the diode-clamped, cascaded H-bridge, T-type, and flying capacitor (FC) type [7]. Among them, the flying capacitor converter (FCC) has the advantage compared to other circuit topologies in terms of its high power density because it does not require an additional power supply circuit or clamping diodes [8].

Multilevel FCCs balance the FC voltage by using optimal switching states with several switching states to output the same voltage level [9–10]. This is necessary to properly achieve equally spaced AC voltage with minimal harmonics distortion. After the introduction of conventional multilevel FCC, various modulation schemes have been proposed to improve the voltage waveform. In [11], the number of voltage levels is increased by changing the FC voltage ratio. However, it is not necessarily an appropriate method for output current ripple reduction because it uses carrier phase shift pulse width modulation (CS-PWM) [12]. On the other hand, space vector modulation (SVM) is a capable method for reducing output current ripple [13–14]. When applying the SVM to FCC, the FC voltage is kept balanced by using vectors with redundancy specific to multilevel converters [15]. In [16], the SVM strategy had been proposed to change the FC voltage ratio, which introduced an increase in output voltage levels. However, the FC voltage ratio must be fixed and not freely changed. Moreover, there is the issue of increased switching frequency to maintain the FC voltage in a control period, resulting in increased switching ripple and lower efficiency.

This paper proposes a novel SVM strategy to reduce the output current ripple by maintaining the unbalanced FC voltage. In the SVM, the voltage levels are increased from three to four, and the additional voltage levels can be freely changed, not limited to 1/2 or 1/3 of the DC voltage, without changing the circuit structure of the three-level three-phase FCC. This allows the build of a space vector diagram that reduces the output current ripple compared to the one of the three-level inverter. To preserve this capable space vector diagram, the proposed SVM scheme is adjusted to maintain the FC voltage unbalanced. The FC voltage unbalance maintenance is adjusted only within a defined region based on the FC charge/discharge reference. The current ripple is reduced by selecting the nearest voltage vector from the FC voltage-sustainable vectors. The current output harmonics reduction and efficiency improvement will be demonstrated by simulation and an experiment with a 7-kW prototype.

II. STRUCTURE OF A THREE-LEVEL FCC

Fig. 1 shows the circuit diagram of the three-level FCC. Each phase has four switching devices ($S_{x1}, S_{x2}, \overline{S_{x2}}, \overline{S_{x1}}$) and a flying capacitor C_x, where $x = u, v, w$ [8]. The proposed strategy increases the output voltage level by maintaining the unbalanced voltage of the flying capacitors in each phase without changing the circuit topology.

A. Basics of Operation of a Three-level FCC

Fig. 2 shows the operating modes of one phase in each switching state. When the upper switches S_{x1} and S_{x2} are turned on, as in Fig. 2(a), the output voltage is equal to the DC

voltage, and when S_{x1} and S_{x2} are turned off, as in Fig. 2(d), the output voltage is zero. When S_{x1} is turned on, and S_{x2} is turned off, as in Fig. 2(b), the FC voltage is applied to the output voltage, and when S_{x1} is turned off and S_{x2} is turned on , as in Fig. 2(c), the output is the voltage subtracted from the DC voltage by the FC voltage. The relationship between switching and output voltage is shown in Table 1.

Generally, the FC voltage is balanced at half the DC voltage. Thus, the phase voltages due to switching states 1 and 2 in Table 1 are the same value at half the DC voltage. The space vector diagram is shown in Fig. 3 (a). The number of voltage vectors is 19 when redundant vectors are excluded. On the other hand, FC voltage is maintained at an unbalance of 40% of DC voltage in the proposed SVM strategy, so that the values of phase voltages in switching states 1 and 2 are different. Thus, the voltage applied to the phase voltage has four levels: 0, V_{fc}, V_{dc}-V_{fc}, and V_{dc}. Note that the FC voltage is controlled at around half the DC voltage in order to avoid the

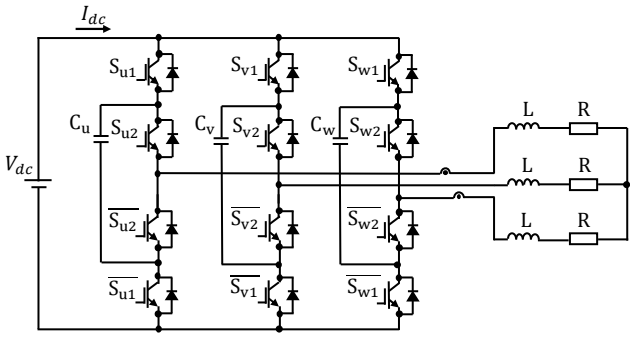
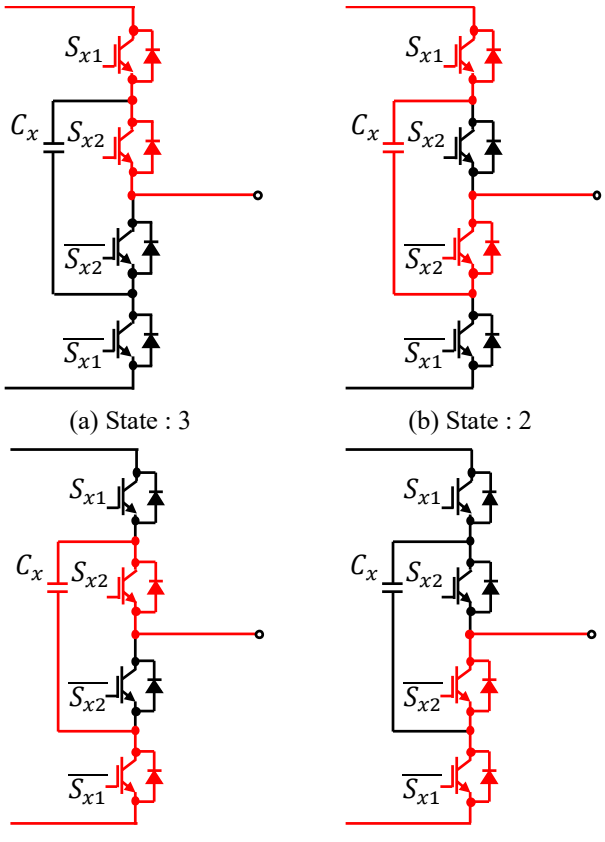


Fig. 1. The circuit diagram of three-level FCC.



(a) State : 3 (b) State : 2

(c) State : 1 (d) State : 0

Fig. 2. Current path of a phase in switching state.

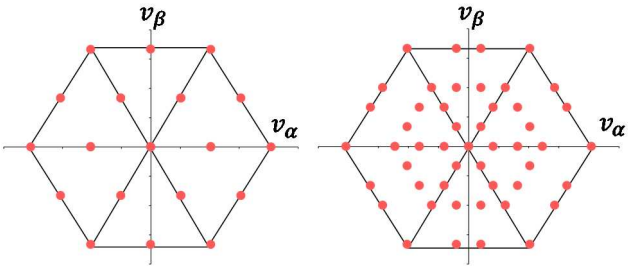
increase in the required voltage rating of switching devices. The number of output vectors on the space vector diagram increases to 49 in Fig. 3 (b). In this way, the output voltage levels are increased by changing the FC voltage ratio. However, unbalancing the FC voltage ratio reduces the number of redundant output voltage vectors, making it challenging to balance the FC voltage to the desired value. In this section, the FC voltage is set at 40% of the DC voltage as an example, but this voltage can be selected freely within the device breakdown voltage.

B. SVM for a Three-level FCC

In this section, the conventional SVM strategy for balancing FC voltage at half the DC voltage is presented. Fig. 4 shows the space vector diagram of a three-level FCC. As with a general two-level inverter SVM, modulation is based on six sectors. The space vector diagram of a three-level FCC features 64 distributed voltage vectors, consisting of a two-layer hexagon placed at the origin of the alpha-beta voltage

TABLE 1 Relation between switching states and voltage levels of three-level three-phase FCC.

States	$\mathbf{S}(S_{x1}, S_{x2}, \overline{S_{x2}}, \overline{S_{x1}})$	$\mathbf{V}_x$
3	S (1, 1, 0, 0)	V_{dc}
2	S (1, 0, 1, 0)	V_{dc} -V_{fc}
1	S (0, 1, 0, 1)	V_{fc}
0	S (0, 0, 1, 1)	0



(a) $V_{fc} = 0.5 \times V_{dc}$. (b) $V_{fc} = 0.4 \times V_{dc}$

Fig. 3. Space vector diagram with changing flying capacitor voltage. The imbalance of FC voltage increases in the number of output voltage vectors.

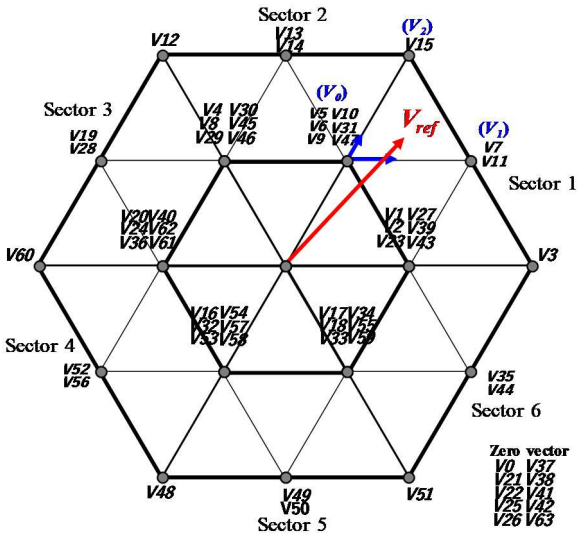


Fig. 4. Space vector diagram of three-phase three-level FCC showing voltage vectors and voltage reference.

axis. Among them, 54 voltage vectors are redundant, and there are 19 basic voltage vectors. These 19 basic voltage vectors are used to control output voltage and 54 redundant voltage vectors are used for FC voltage balancing. When the voltage reference $\boldsymbol{V}_{ref}$ in the region of sector 1 is given in Fig. 4, $\boldsymbol{V}_{ref}$ is decomposed into the voltage components V_0, V_1 and V_2 and output during T_0, T_1, T_2 of the control period T_s in equation (1).

$$\begin{aligned} \boldsymbol{V}_{ref} \cdot T_s &= \boldsymbol{V}_0 T_0 + \boldsymbol{V}_1 T_1 + \boldsymbol{V}_2 T_2 \\ T_s &= T_0 + T_1 + T_2 \end{aligned} \quad \cdots\cdots (1)$$

Six redundant vectors output $\boldsymbol{V_0}$ and two output $\boldsymbol{V_1}$ when adjacent vectors are selected for the voltage reference in Fig. 4. Then, the cost function is defined with respect to the vector with redundancy, and redundancy vectors at the same coordinates are optimally selected by feedback of the FC voltage and the output current [13].

III. Proposed SVM Strategy

In this section, the proposed SVM method for changing the FC voltage ratio is described. Fig. 5 shows the space vector diagram when the FC voltage is maintained at 40% of the DC voltage as an example. The redundant fundamental vectors in Fig. 4 are split and placed on the four hexagons (Hex1 to Hex4) and at the origin by unbalancing the FC voltage. Thus, the number of voltage vectors increases to 49. However, the FC voltage is not maintained by the conventional SVM scheme because the number of switching states of the redundant voltage vectors is decreased. The proposed SVM method performs the optimal selection of three vectors to achieve the following two objectives:

(i) Maintain unbalanced FC voltage.

(ii) Minimize output voltage and current ripple.

Three vectors are selected to achieve the above two objectives, and the output periods T_0, T_1, and T_2 of each vector are calculated from equation (1) to allocate the voltage reference $\boldsymbol{V}_{ref}$. For example, given the voltage reference $\boldsymbol{V}_{ref}$ in the region of sector 1 in Fig. 5, when the vectors $\boldsymbol{V_0} = \boldsymbol{V9}$ (020), $\boldsymbol{V_1} = \boldsymbol{V15}$ (230), and $\boldsymbol{V_2} = \boldsymbol{V7}$ (210) are selected based on the above objectives, the gate signals of the inverter are generated as in Fig. 6. Here, the numbers in parentheses represent the switching states of the vectors based on Table 1. The vector selection strategy will be explained in the next subsection.

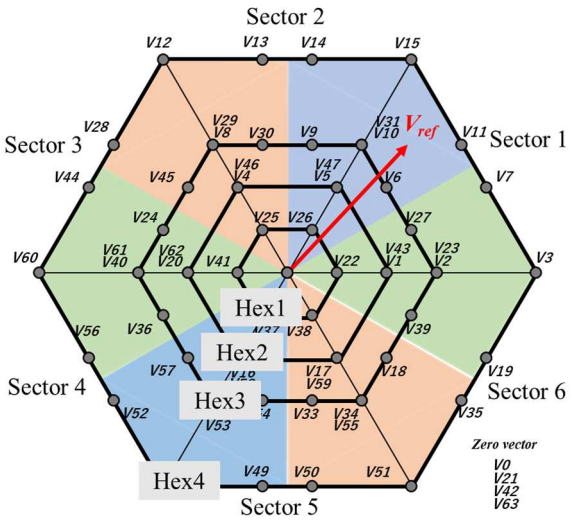


Fig. 5. Space vector diagram for three-phase three-level FCC with unbalanced FC voltage. Four hexagon show regions of charge/discharge of FC.

The background color in Fig. 5 indicates the region of maximum absolute phase current with the unity power factor. The U-phase current is maximum from -30° to 30° and 150° to 210°. The V-phase current is maximum from 30° to 90° and 210° to 270°. The W-phase current is maximum from 90° to 150° and 270° to 330°. The modulation method is presented in detail in the next section using the region divided in this section.

A. Vector Selection for Maintaining FC Voltage Unbalance

The FC voltage unbalance maintenance is based on the FC charge/discharge reference Q^*_{fc}. The FC charge/discharge reference is

$$Q^x_{fc} = \begin{cases} 1 & \text{if } v^x_{fc} < v^*_{fc} \\ 0 & \text{if } v^x_{fc} = v^*_{fc} \\ -1 & \text{if } v^*_{fc} < v^x_{fc} \end{cases} \quad \text{for } x \in \{u, v, w\} \quad \cdots\cdots (2)$$

and is calculated based on FC voltage feedback v^x_{fc} and FC voltage reference v^*_{fc}. FC charge/discharge references are calculated for FCs on each phase in each control period: "1" represents the charging command, "0" represents either charge or discharge is allowed, and "-1" represents the discharging command.

The variation range of FC voltage during a control period is calculated by the following :

$$\Delta v^x_{fc} = \frac{1}{C_{fc}} \int i^x_{fc}(t)\, dt \quad \cdots\cdots (3)$$

where C_{fc} is the capacitance of the FC. Eq. 3 indicates that the amplitude and direction of the FC current must be known in order to charge and discharge the FC. The FC current is calculated based on the switching states S_{x1} and S_{x2} of the x-phase legs and the output phase current i_x by the following equation :

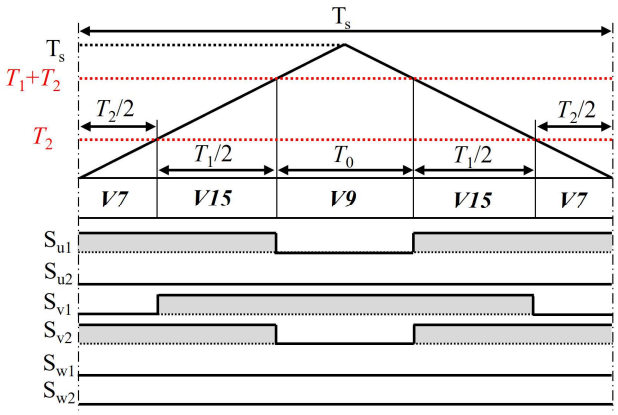


Fig. 6. Gate signal generation to output voltage reference from the output period of the three vectors.

$$i_{fc}^{x} = \begin{cases} i_x & \text{if } S_{x1}=0,\ S_{x2}=1 \\ -i_x & \text{if } S_{x1}=1,\ S_{x2}=0 \end{cases} \text{ for } x=\{u,v,w\} \quad \cdots\cdots (4).$$

The FC current passes through three current paths in a control period by the three selected vectors. The FC voltage variation during a control period is thus the sum of the voltage variations due to the three different FC currents. In the proposed SVM, the FC voltage variation in a control period is to be kept within 5% of the supply voltage from the point of reduction of the voltage error in the space vector diagram.

The following discusses the selection of voltage vectors, taking into account the FC voltage variations described earlier. Within the control period, there are three voltage vectors to be selected: the base vector $\boldsymbol{V_0}$, the first vector $\boldsymbol{V_1}$, and the second vector $\boldsymbol{V_2}$. The base vector $\boldsymbol{V_0}$ is used for vector selection to maintain FC voltage unbalance. As discussed before, the background color in Fig. 5 is the area with the maximum absolute value of the phase currents with a unity power factor. This area has the most influence on FC voltage because the instantaneous output current of the corresponding phase is the maximum according to Eq. (3). Thus, the base vector $\boldsymbol{V_0}$ is selected to be the vector that satisfies the FC charging/discharging reference in equation (1) only for an FC of the phase with the highest output current. For example, consider the voltage reference in Fig. 5 and the FC charging/discharging reference in (5). In this case, the FCs of phases U and W need to be charged, while the FC of phase V needs to be discharged. As a result, the base vector $\boldsymbol{V_0}$ is selected as a vector to charge the FC of phase W so that the voltage reference is in the highest region of phase W.

$$\{Q_{fc}^{u},\ Q_{fc}^{v},\ Q_{fc}^{w}\} = \{1, -1,\ 1\} \quad \cdots\cdots (5)$$

The other vectors, $\boldsymbol{V_1}$ and $\boldsymbol{V_2}$, are selected to minimize ripple, without affecting the charging and discharging processes. This will be discussed in the next section. Hex2 in Fig. 5 is classified into the discharge vector group because the voltage vectors due to state 1 in Table 1 are distributed, and Hex 3 is classified into the charge vector group because the voltage vector due to state 2 is distributed. From the above, only $\boldsymbol{V_0}$ is selected from Hex3, and $\boldsymbol{V_1}$ and $\boldsymbol{V_2}$ are selected from all hexagon groups.

B. Vector Selection for Output Current Ripple Minimization

There are some voltage vectors in a sector that achieve the previous section. First, the output times T_0, T_1, and T_2 of the selected voltage vectors must satisfy the voltage reference,

$$0 < T_i \quad \text{for } i \in \{0,1,2\} \quad \cdots\cdots (6)$$

must be satisfied. To select the final three vectors, choose the voltage vector that achieves Eq. (2) with the lowest output voltage and current ripple. The three vectors must be closed to the voltage reference to reduce the output voltage and current ripple. Thus, the lengths of the lines l_0, l_1, and l_2 are calculated by connecting the voltage reference and each vector, and vectors with the smallest total L are selected to reduce the output voltage and current ripple. The length l_0, l_1, l_2, and L are calculated as follows:

$$l_0 = \sqrt{(v_{0\alpha} - v_{\alpha}^{*})^2 + (v_{0\beta} - v_{\beta}^{*})^2} \quad \cdots\cdots (7),$$

$$l_1 = \sqrt{(v_{1\alpha} - v_{\alpha}^{*})^2 + (v_{1\beta} - v_{\beta}^{*})^2} \quad \cdots\cdots (8),$$

$$l_2 = \sqrt{(v_{2\alpha} - v_{\alpha}^{*})^2 + (v_{2\beta} - v_{\beta}^{*})^2} \quad \cdots\cdots (9),$$

$$L = l_0 + l_1 + l_2 \quad \cdots\cdots (10),$$

where $v_{0\alpha}$, $v_{0\beta}$ are the coordinates of $\boldsymbol{V_0}$, $v_{1\alpha}$, $v_{1\beta}$ are the coordinates of $\boldsymbol{V_1}$, $v_{2\alpha}$, $v_{2\beta}$ are the coordinates of $\boldsymbol{V_2}$, and v_{α}^{*}, v_{β}^{*} are the coordinates of the voltage reference.

IV. Evaluation of Proposed SVM to Maintain Unbalanced FC Voltage

A three-level FCC is simulated to evaluate the proposed SVM scheme and to understand how the unbalanced FC voltage is maintained and how the different FC voltage ratio affect the switching ripple. The proposed SVM is implemented, as shown in Fig. 7. When FC voltage is maintained unbalanced, the voltage vectors on the space vector diagram change position with FC voltage variation. The changes in vector position cause output voltage errors and THD deterioration. The space vector diagram should be redrawn at each control period. However, the computation load on the DSP increases due to redrawing of all the vectors. Thus, the space vector diagram is redrawn only at a sector with the voltage reference to reduce the computation load, and vector selection is performed within the redrawn sector. Confirm the results by simulating the operation of the proposed SVM scheme using the circuit configuration in Fig. 1. Table 2 shows the parameters used in the simulation.

A. FC Voltage Unbalance Effect

Simulation is performed by unbalancing the FC voltage at 40% of the DC voltage to confirm that the FC voltage is maintained unbalancing. Fig. 8 shows the current and FC voltage waveforms of the three-level FCC with the proposed SVM strategy. The FC voltage is maintained at 120 V unbalanced at the voltage reference. The proposed SVM

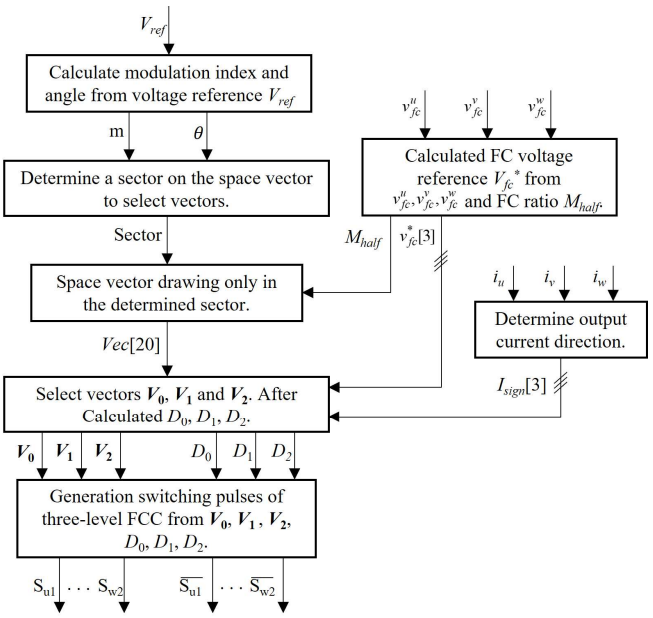


Fig. 7. Flowchart of the proposed SVM scheme to unbalance FC voltage.

TABLE2 Rated values and parameters of three-level FCC.

System parameter		Value	
Output Power	P_{out}	7	kW
Input Voltage	V_{dc}	300	V
Switching Freq.	f_s	10	kHz
Output Freq.	f	50	Hz
Load Inductance	L	0.346	mH
Flying Capacitor	C_{fc}	500	μF
FC Voltage Ref.	V_{fc}^*	120	V
Modulation Index	M	0.82	-

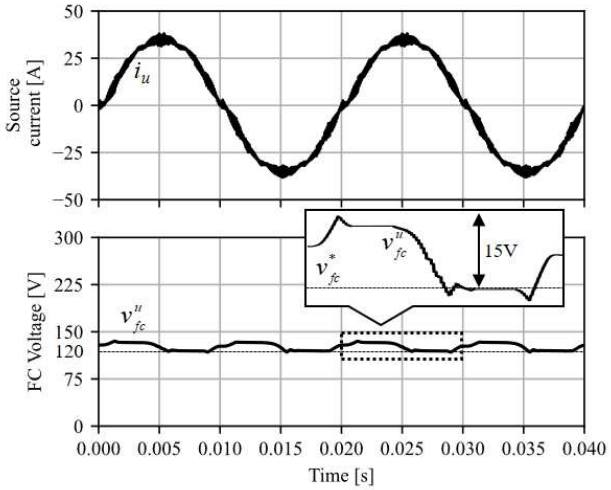


Fig. 8. Output current and FC voltage with proposed SVM when FC voltage is maintained unbalanced at 120 V.

allows the maximum variation of FC voltage to be below 15 V, which is within 5% of the DC voltage. As a result, the phase currents provide a sinusoidal as referenced, without the error in the voltage vector significantly affecting the output current waveform.

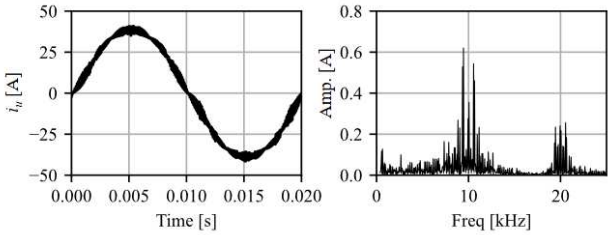
B. Switching Ripple Reduction Effect

The effect of different FC voltage ratios on switching ripple is confirmed. Figs. 9 (a) and (b) show the output current waveforms and FFT analysis results of the conventional balanced SVM method applied to a three-level FCC. In addition, Fig. 10(a) and Fig. 10(b) show the output current waveforms and results of the FFT analysis under the unbalanced condition by the proposed SVM method. Note that both waveforms show only the U-phase current. The proposed SVM makes the output current sinusoidal, with FC voltage maintained unbalanced. Harmonics the switching component was suppressed by 26% using the proposed SVM, which was confirmed by the FFT analysis results. From this, the proposed SVM is effective in reducing the switching ripple of the output current.

V. EXPERIMENTAL RESULTS

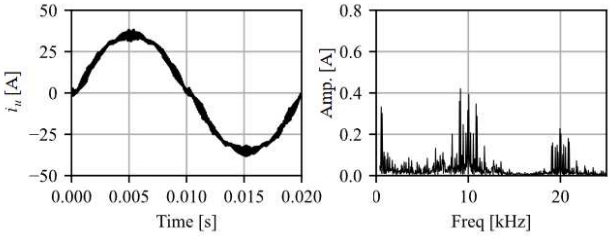
Experimental tests were performed with a 7-kW prototype of a three-level FCC in Fig. 11. The inverter was controlled by a DSP TMS320F283790 and an FPGA SPARTAN-7. Table 3 shows the parameters. The load power factor was set to 1 and the modulation factor was set to 0.82 in the experiment.

Fig. 12(a) shows the output line-to-line voltage and phase currents when the FC voltage is maintained at 50% of the DC



(a) (b)

Fig. 9. Simulation waveforms of the proposed SVM scheme maintaining V_{fc} at 50% of the DC voltage. (a) is U-phase current. (b) is FFT analysis result for U-phase.



(a) (b)

Fig. 10. Simulation waveforms of the proposed SVM scheme maintaining V_{fc} at 40% of the DC voltage. (a) is U-phase current. (b) is FFT analysis result for U-phase.

TABLE 3 Experimental system parameters.

System parameter	Value
Switching devices	IGBT 2MBI50N-060
DC source voltage (V_{dc})	300 V
Capacitance of DC (C_{dc})	4.7 mF
Capacitance of FCs (Cu, Cv, and Cw)	1.8 mF
Switching Freq.	10 kHz
Output Freq.	50 Hz
Load-Resistance and Inductance (R, L)	5.5 Ω, 346 mH

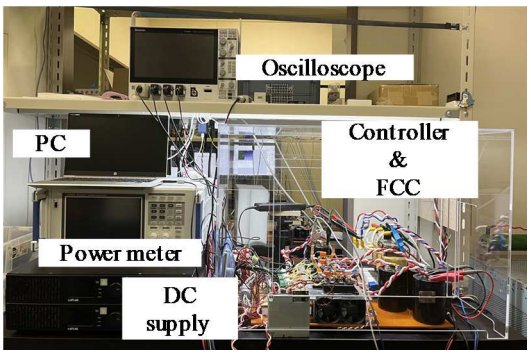
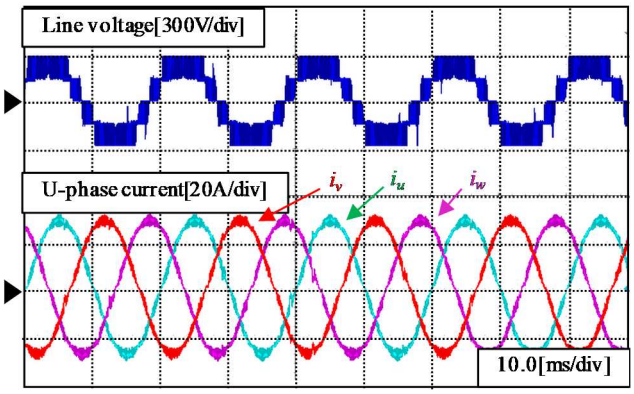
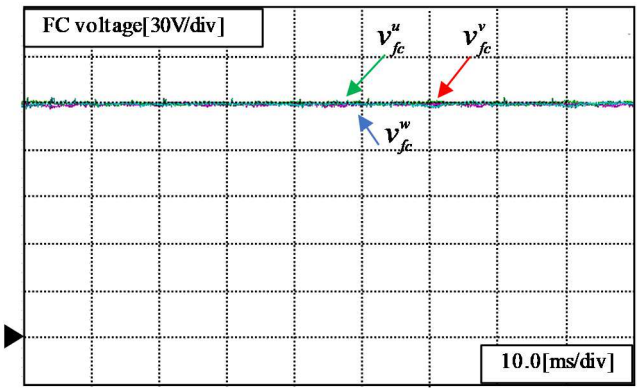


Fig. 11. Experimental setup.

voltage with the proposed SVM strategy. As can be seen in Fig. 12(a), there are five levels in the line voltage. Each FC voltage is maintained to be balanced at 150 V as in Fig. 12(b). Fig. 13 shows the output line-to-line voltage, phase currents, and FC voltages when the FC voltage is unbalanced at 40% of the DC voltage by the proposed SVM scheme. Fig. 13(a) shows that the number of levels of line voltage can be increased to seven levels by the proposed SVM scheme. Fig. 13(b) shows that the FC voltage is regulated at 120V, confirming that the unbalance can be maintained. Fig. 14

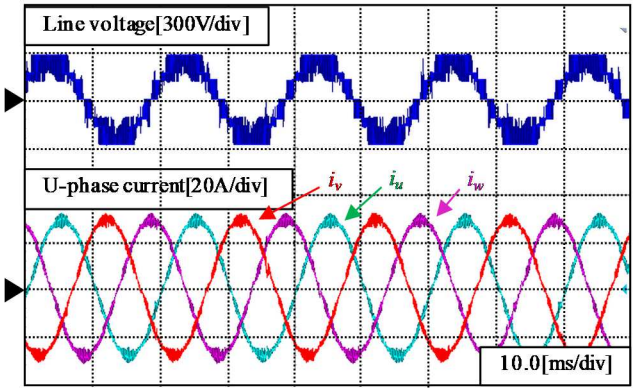


(a)

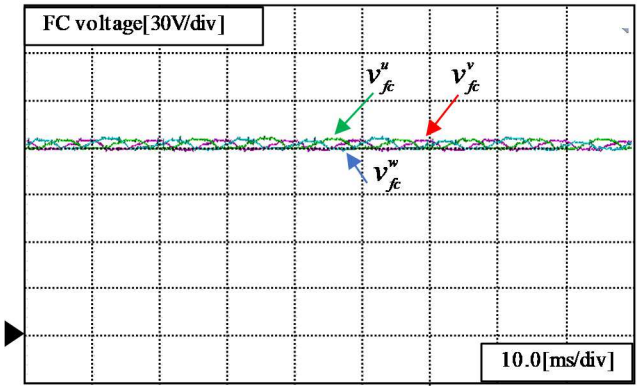


(b)

Fig 12 Experimental results of the proposed SVM scheme to maintain FC voltage at 150V. (a) line voltage and three-phase currents. (b) three-phase FC voltages.

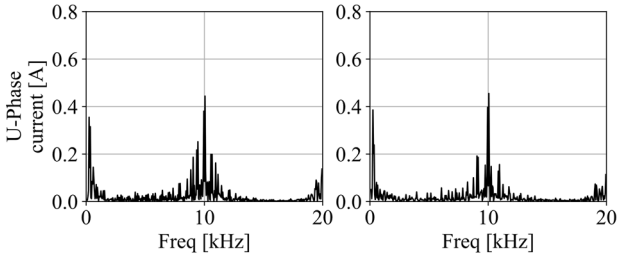


(a)



(b)

Fig 13 Experimental results of the proposed SVM scheme to maintain FC voltage at 120V. (a) line voltage and three-phase currents. (b) three-phase FC voltages.



(a) (b)

Fig.14 FFT analysis of experimental output U-phase current. (a) maintains FC voltage at half the DC voltage (50 V). (b) maintains FC voltage at 40% of DC voltage (120 V).

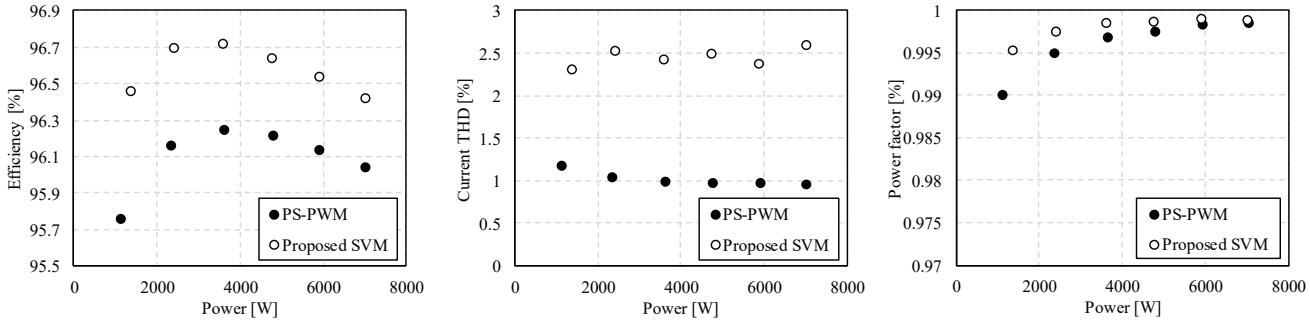
shows the phase current FFT results for balanced and unbalanced conditions. The proposed unbalanced SVM scheme reduces the harmonics of the switching frequency component greatly and the ripple of the output phase currents in Fig. 14.

To analyze the performance of the proposed SVM scheme, experiments were conducted under a wide range of operating conditions with the FCs unbalanced at 40% of DC voltage. The analyses are performed by measuring the inverter efficiency and current THD (up to 40th order) and load power factor. The output power ranged from 1kW to 7kW, and the modulation ratio was set to 0.82. Note that CS-PWM, which is commonly used in general, was employed for comparison. The switching frequency for both modulations was set to 10 kHz in common. Table 2 shows the various parameters for the test. Fig. 15(a) shows the efficiency curves, which are improved by more than 0.3 points at all operating points with the proposed SVM schemes, achieving a maximum of 0.7 points. Fig. 15(b) shows the current THD, which is worsened by the proposed SVM scheme. This can be improved over the conventional method with appropriate dead-time compensation. However, THD is kept within 4% at all operating points. The power factor comparison in Fig. 15(c) confirms the superiority of the proposed SVM scheme at all operating points.

Finally, Fig. 16 shows a comparison of efficiency with unbalanced FC voltages of 90–210V. The result in Fig. 16 shows the efficiency when the FC voltage is maintained in the range of 30–70% of the DC voltage, and the proposed SVM scheme improves the efficiency. This is unbalancing the FC voltage rather than balancing it requires fewer switching counts and results in lower switching losses.

VI. CONCLUSION

This paper presents a novel space vector modulation (SVM) strategy to reduce output current ripple without change in circuit topology for the three-level flying capacitor converter. The proposed SVM scheme sets the flying capacitor voltage to neither 1/2 nor 1/3 of the DC voltage, allowing for more flexible voltage determination. Moreover, maintaining the FC voltage unbalanced increases the number of selectable voltage vectors, thereby reducing switching ripple. The modulation objectives of the proposed SVM scheme are the following.



(a) (b) (c)

Fig. 15. The relationship curves between output power and (a) efficiency, (b) current THD, (c) power factor for proposed SVM scheme.

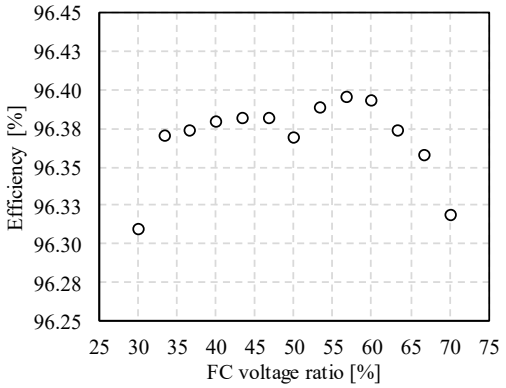


Fig. 16. Experimental results of efficiency for different maintained FC voltage in the proposed SVM scheme.

(a) Maintained unbalanced FC voltage.

(b) Minimum output current ripple.

Experiments using a 7-kW inverter demonstrated that the proposed SVM scheme reduces the carrier harmonics component. Additionally, it was confirmed that the proposed modulation improves the converter efficiency by 0.7 points.

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