Paper

Single-Phase AC Grid-Tied Inverter with Buck-Type Active Power Decoupling Circuit Operated in Discontinuous Current Mode

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This study presents a novel circuit topology for a single-phase inverter using an active power decoupling circuit operated in discontinuous current mode (DCM). In a conventional single-phase grid-tied inverter, bulky capacitors are used in a DC-link to absorb a power ripple with twice the grid frequency. However, electrolytic capacitors limit a converter's lifetime. In contrast, ceramic capacitors are used in the proposed circuit since the required capacitance is reduced. Furthermore, the active power decoupling circuit in DCM has no inductor inside by utilizing the current zero cross featured in DCM for power ripple compensation modes. An experimental verification using a 1-kW prototype shows a 90.2% current ripple reduction caused by the power ripple with twice the grid frequency. The efficiency exceeds 94% in the 20% region of the rated power to 1-kW through 96.0% of the 650 W maximum. According to a theoretical evaluation using a Pareto-front optimization assumed as a 3-kW system, the proposed circuit reaches the maximum power density at 20 kHz which is 115 % higher than that of the passive power decoupling method. The inductor volume in the proposed circuit is reduced by 30.4% compared to a conventional buck-type active power decoupling circuit.

Keywords : Single-phase inverter, Discontinuous current, Power density, Power decoupling;

1. Introduction

In recent years, power conversion systems (PCSs) for a DC to single-phase AC grid has been studied actively for photovoltaics systems or battery energy storage systems and so on [1-3]. In the single-phase grid, an instantaneous power oscillates at twice the grid frequency, whereas the PV output power requires constant power for achieving higher maximum power point tracking (MPPT) efficiency. As a result, the power ripple with twice the grid frequency is needed to be compensated in the PCSs. However, a lifetime of the PCSs is limited in a conventional passive method using bulky electrolytic capacitors, according to Arrhenius law [4].

As alternative compensation methods, active power decoupling circuits have been proposed [5-9]. In the active power decoupling circuits, the power ripple is absorbed by average stored energy $C\Delta V^2/2$ of buffer capacitors with large voltage oscillation ΔV . As a result, a longer lifetime of the PCSs is expected since the film or ceramic capacitors can be used. In recent years, not only high-efficiency conversion but also high-power density is especially required to the PCSs [10-13]. However, the active power decoupling circuits are suffering from the low power density due to the additional components, especially the inductors. Although the required inductance can be reduced by increasing switching frequency, a trade-off between the inductor volume and the cooling system count on the semiconductor switching loss, especially in a boost-type active power decoupling circuit needs high voltage

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rating semiconductors [14].

This study proposes a new buck-type active power decoupling circuit characterized by no additional inductor in the circuit. The proposed active power decoupling circuit utilizes discontinuous current mode (DCM) to absorb the power ripple. The proposed circuit achieves two operations independently with one boost inductor by applying DCM. The high-power density is expected in comparison with the conventional active power decoupling circuits because the additional inductor is not necessary for the proposed active power decoupling circuit. Furthermore, high efficiency is also expected since the semiconductor with a low on-resistance rating is used. This paper is organized as follows. Firstly, in the second section, the features of conventional active power decoupling methods and the proposed active power decoupling circuit are introduced. Secondly, the operation principle of the proposed active power decoupling circuit is explained based on a control strategy. Thirdly, the proposed active power decoupling circuit is verified by an experiment using a 1-kW prototype. Finally, theoretical evaluations using a Pareto-front optimization compare the efficiency and the power density among a passive power decoupling method, several conventional active power decoupling circuits, and the proposed active power decoupling circuit in DCM.

2. Active Power Decoupling circuits

In this section, the mechanism of a power ripple caused in DC to single-phase AC converters is explained at first.

2.1 Principal of active power decoupling

Figure 1 shows the relation among the input power p_{in} , the output power p_{out} and the compensation power p_{buf} in the DC to single-phase AC converter. The instantaneous output power is shown in

(1) when the output current is sinusoidal wave with unity power factor.

where V_m is the peak voltage of the single-phase grid, I_m is the peak current of the inverter output, and ω_{out} is the angular frequency of the grid. The power ripple with twice the grid frequency occurs in the DC-link because the input power is controlled to a constant value for high MPPT efficiency. In order to absorb the power ripple, the instantaneous compensation power p_{buf} is controlled according to

$$p_{buf} = \frac{V_m I_m}{2} \cos\left(2\omega_{out}t\right) \dots (2).$$

As a result of the energy charge or discharge of the buffer capacitor, the input power p_{in} is controlled to the constant value of the average value of (1). The capacitance of the power decoupling circuit is decided from a relation between the storage energy and the capacitor voltage. From the instantaneous power in (2), the storage power of the buffer capacitor is represented by

where v_{ave} is the average voltage, and Δv_c is the voltage oscillation range of the buffer capacitor. In a passive power decoupling method using bulky electrolytic capacitors, the power storage energy in (3) is satisfied with large capacitance. By contrast, the active buffers apply larger voltage amplitude Δv_c with smaller capacitance to the power storage energy. Therefore, a long lifetime system is realized by using film or ceramic capacitors in the active power decoupling circuits.

2.2 Passive power decoupling method with electrolytic capacitors

Figure 2 shows a passive buffer topology applied to a DC to single-phase AC grid-tied connected inverter. This topology consists of a boost chopper, bulky capacitors, and a voltage source single-phase inverter (VSI). However, the electrolytic capacitors limit a lifetime of the converter according to the Arrhenius law [14].

2.3 Conventional active power decoupling circuits

Figure 3 shows a circuit configuration of a single-phase inverter with a conventional boost-type active power decoupling circuit. In this active power decoupling circuit, the boost chopper with the buffer capacitor C_{buf} to absorb the power ripple is connected to the VSI in parallel. The active power decoupling circuit obtains a longer lifetime because the film or ceramic capacitors are used to the buffer capacitor. However, additional components are necessary to control the capacitor voltage. The additional inductor especially tends to cause lower power density. The volume of a cooling becomes larger due to the increase of switching loss, especially in the boost chopper requiring the semiconductors with high rating voltage, when the high switching frequency is required to reduce the inductor storage energy.

Figure 4 shows a circuit configuration of a conventional bucktype active power decoupling circuit. The semiconductors with lower rating voltage are used because the buffer capacitor voltage is controlled to smaller than the DC-link voltage. However, this topology also needs additional inductor in the active power decoupling circuit. As a result, the active power decoupling circuit is suffered from the power density reduction due to the additional components, especially the inductor.

2.4 Buck-type active power decoupling circuit operated in discontinuous current mode

The discharge mode for the buffer capacitor C_{buf} is not realized due to the impossibility of changing the current direction suddenly, when the DC-DC converter operates in CCM. Thus, this paper came up with the idea that the charge and the discharge are realized by DCM. By utilizing the zero-current period of the DCM, the input voltage is pushed up to the DC-link voltage, and stepped down to the buffer capacitor voltage through only one boost inductor [15].

Figure 5 shows a circuit configuration of the proposed buck-type active power decupling circuit operated in DCM. The proposed active power decupling circuit in DCM is integrated in the DC-DC conversion stage without no additional inductors. By the additional



Fig. 1. Schematic power relation among input, output and buffer.



Fig. 2. DC to single-phase AC converter with passive power decoupling method with electrolytic capacitors.







Fig. 4. Conventional buck-type active power decoupling circuit.

bidirectional switch S₄, the short connection between C_{buf} and C_{dc} is avoided. The additional switches require the devices with low rating voltage. Therefore, the proposed active power decoupling circuit achieves a high conversion efficiency.

3. Operation Principle of Proposed Active Power Decoupling Circuit in DCM

This section explains an operation principle of the proposed active power decoupling circuit in DCM. The operation modes and the control strategy of the power ripple compensation are described.

Figure 6 shows operation modes of the buck-type active power decoupling circuit. The proposed converter has the four operation modes; Mode 1 and 2 for the boost chopper operation, and Mode 3 and 4 for the active power decoupling operation. It is characterized that the proposed converter must be operated in DCM to share the boost inductor L_{boost} for these controls.

Figure 7 shows the current waveforms of the boost inductor for the capacitor charging operation and the discharging operation. In Mode 1 and 2, the converter boosts the input voltage to the DC-link voltage. Mode 1 and 2 are the typical boost operation irrespective of the charging and discharging operation of the buffer capacitor. The buffer capacitor voltage is controlled in Mode 3 and 4. The charging mode and the discharging mode of the buffer capacitor is switched by changing the order of Mode 3 and 4. The boost chopper operation and the active power decoupling operation time-share the boost inductor. In order to avoid the interference between the boost chopper operation and the active power decoupling operation, the inductor current must have a zero-current period between these controls. For this reason, the proposed converter must be operated in DCM.

Note that the proposed converter has a limitation on the relationship among the input voltage, buffer capacitor voltage, and DC-link voltage to avoid the short circuit. The buffer capacitor voltage must be larger than the input voltage v_{in} and must lower than the DC-link voltage, as shown in

 $v_{in} < v_{buf} < v_{dc}$ (4).

3.1 Mode 1

In the Model, the current is flowing to the boost inductor L_{boost} from the DC-side, when the switching devices S₁ is turned on. The inductor current starts to increase from zero. Moreover, the flowing current for the buffer capacitor is zero because the between of the active power decoupling circuit and the input side is closed-off by using a bidirectional switching devices S₃ and S₄. The buffer capacitor voltage and the DC-link voltage are kept in the values at the starting value of this mode.

3.2 Mode 2

The switching devices S_2 turns on, and S_1 turns off. In Mode 2, the energy of the boost inductor is transferred to DC-link. The buffer capacitor voltage is continuously kept in the constant value, and the current for the buffer capacitor is zero.

In this mode, the inductor current must reach zero for the preparation for avoiding the interference between the Mode 1 and 2, and Mode 3 and 4.

3.3 Mode 3

The Mode 3 and 4 are used for the active power decoupling. The buffer capacitor voltage is controlled by the combination of the switches of S_1 , S_3 , and S_4 . In the proposed method, the additional



Fig. 5. Buck-type active power decoupling circuit operated in discontinuous current mode.



Fig. 6. Operation modes.





inductor is not necessary for the active power decoupling. Because the instantaneous current at the start of Mode 3 is always zero by the DCM operation, the active power decoupling operation is as same as the boost chopper with DCM.

1) Buffer capacitor charging operation

In Fig. 7 (a), for charging the buffer capacitor, the S_1 is firstly turned-on and achieves ZCS. The necessary energy for the active power decoupling operation is transported from the input side to the boost inductor in this buffer capacitor charging operation. Note that the input current in this mode is not flowing to the buffer capacitor because the buffer capacitor voltage is higher than the input voltage at all time. The voltage of the buffer capacitor is kept in the constant value in this mode.

2) Buffer capacitor discharging operation

By contrast, when the S_3 is firstly turn-on, the buffer capacitor discharges, as shown in Fig. 7 (b). Mode 3 continues until the inductor current reaches zero to avoid the interference between the boost chopper operation and the active power decoupling operation.

3.4 Mode 4

The current of the active power decoupling circuit is only flowing in this Mode 4.

1) Buffer capacitor charging operation

In Fig. 7 (a), when the S_3 is turned-on after Mode 3, the buffer capacitor voltage increases in order to compensate the twice ringing component caused by connecting single-phase load. The period with zero inductor current allows the buffer capacitor charging operation: Mode 4.

2) Buffer capacitor discharging mode

In the buffer capacitor discharging operation, as shown in Fig. 7(b), the converter firstly operates in Mode 4 in the active power decoupling operation. The discharging operation of Mode 4 is presented by the period from the zero to the current peak of the active power decoupling operation i_{peak} . Note that the peak current i_{peak} is determined by the compensation current reference i_{buf} of the twice the grid frequency component in both charging or discharging operation.

3.5 Calculating equations of each current

The average current i_{L_ave} of the boost inductor is the sum of the average current for the DC-link voltage control $i_{L_ave_de}$ as Mode 1 and 2, and the buffer capacitor voltage control $i_{L_ave_buf}$ as Mode 3 and 4.

Each average current of these modes is controlled by using the common inductor L_{boost} independently.

1) Boost operation

The necessary current for the transported power to DC-link is given by

$$i_{L_ave_dc} = \frac{i_{peak}}{2} (d_1 + d_2) \dots (6)$$

where d_1 and d_2 are the on-duties of S₁ and S₂, and i_{peak} is the current peak of the boost operation. The peak current i_{peak} and each duties d_1 and d_2 of the boost operation is constant value by decided the transported power.

2) Active power decoupling operation

In order to control the average current of the boost inductor to a constant without the ripple component, $i_{L_ave_buf}$ is given by

$$i_{L_ave_buf} = \frac{i_{peak}}{2} (d_3 + d_4)$$
(7),



Fig. 8. Control strategy of DC link voltage and buffer capacitor voltage.

where d_3 and d_4 are on-duties of S₁ and S₃, i_{peak} is the current peak of the buffer capacitor voltage control. These duties d_3 and d_4 of the compensation operation for the ripple component are decided PI controller. As a result, according to (6) and (7), the average current of boost inductor is controlled at the constant value.

3.6 Control strategy

Figure 8 shows the voltage control block diagram for the DC-link and the buffer capacitor in the active power decoupling circuit in DCM. The proposed control method consists of the current control of the boost inductor as miner loops. The authors have demonstrated that the DCM current control achieves the same current control bandwidth of the CCM current control by eliminating the nonlinearity in the DCM current control [16]. Based on this concept, the current control of the boost inductor is also designed as the CCM current control in the active power decoupling circuit in DCM. Moreover, the DC-link voltage and the buffer capacitor voltage is controlled by the current on the common inductor because the zerocurrent period in the DCM is inserted in order to separate each voltage control, as shown in Fig. 7.

1) DC-link capacitor voltage control

In Fig. 8, a voltage command of the DC-link should be higher than the peak voltage of the gird. In addition, a constant DC-link voltage is desirable to improve a THD characteristic of the inverter output current. To control the DC-link voltage, firstly, the inverter output power is calculated from a multiplication between the detected grid voltage and the inverter output current. Then, the calculated result of the inverter output power divided by the detected the DC-link voltage is feedforwarded to an output of a PI controller of the DC-link voltage control. As a result of this feedforward, the voltage ripple with twice the grid frequency is compensated. Therefore, small capacitors are used in the DC-link because the current flowing to the DC-link capacitors includes the only switching frequency components caused by the inverter.

2) Buffer capacitor voltage control

In order to absorb the power ripple, the buffer capacitor voltage is controlled to oscillate at twice the grid frequency. In the proposed control method, an average voltage of the buffer capacitor is given as the voltage reference. Therefore, the automatic voltage regulator (AVR) with high bandwidth is not necessary. The current reference i_{buf}^{*} is inserted to the output of a PI controller to make the capacitor charge or discharge, which is represented by

Rated power	Р	1 kW	
Input voltage	Vin	150 V	
DC-link voltage	<i>v_{dc}</i>	380 V	
Buffer capacitor voltage	v _{buf_ave}	250 V	
	Δv_c	160 V	
Switching frequency	f _{sw}	DC-DC converter : 20 kHz Inverter : 10 kHz	
Capacitance	Cbuf	120 µF (40 µF, 3P), Ceramic	
	C_{f}	54 µF (27 µF, 2P), Ceramic	
Inductance	Lboost	48.7 µH, Ferrite core	
	Lgrid	1.6 mH (%Z=1.5%)	
Switching device	$S_1 \sim S_4$	SiC-MOSFET Rohm, SCH2080KE (S1:3P, S3:2P)	
	$S_{up} \sim S_{wn}$	IGBT Fuji electric, FGW30N60VD	

Table 1. Circuit parameters for 1-kW prototype

$$i_{buf}^{*} = \frac{P}{v_{buf}} \cos(2\omega_{out}t)$$
(8)

where *P* is the rated output power. Finally, the gate signals of S_1 - S_4 are given by a carrier comparison between a saw-tooth waveform and the duties d_1 - d_4 .

4. Experimental Verifications of the Active Power Decoupling Circuit in DCM by using 1-kW Prototype

4.1 Fundamental operation in simulation

The fundamental operation of the proposed circuit in DCM is presented by the simulation.

Table 1 shows the circuit parameters and the components used in the experiments.

1) Fundamental waveforms in simulation

Figure 9 shows the simulation waveforms of the proposed circuit with or without the active power decoupling. Fig. 9 (a) shows a result without the proposed active power decoupling. As shown in Fig. 9 (a), the boost inductor current is distorted by the power ripple component with twice the grid frequency. The proposed circuit has a small capacitance of C_{buf} which is not completely compensated to the power ripple at 100 Hz. In contrast, Fig. 9 (b) shows a result with the active power decoupling. The current ripple caused by the power ripple with twice the grid frequency is reduced in Fig. 9 (b), owing to the proposed active power decoupling.

Figure 10 shows the enlarged waveforms of areas A and B in Fig. 9. Figure 10 (a) shows the buffer capacitor charging mode, whereas Fig. 9 (b) shows the buffer capacitor discharging mode. The boost inductor current is discontinuous, i.e., DCM. As shown in Fig. 10 (a), the first smaller current ripple operates whereas the second current ripple performs the active power decoupling, i.e., the buffer capacitor charging operation. Similarly, as shown in Fig. 10 (b), the positive current performs the active power decoupling, i.e., the discharging operation of the buffer capacitor.

2) Proposed operation under transient state

Figure 11 shows the transient response at the load step with the active power decoupling operation. This test conducted with change in the load from 1 kW to 500 W. Note that the load step is provided by the current source for simplicity. The overshoot voltage of the



(a) W/o active power decoupling (b) With active power decoupling Fig. 9. Fundamental operation waveforms. The boost current waveform with DCM is deiced by the mode of the buffer capacitor voltage.



Fig. 10. Extended current waveform of area A and B in Fig. 9 with power decoupling method using DCM. This figure shows the buffer capacitor in the charging mode as shown in area A and the discharging mode as shown in area B of Fig. 9.



Fig. 11. Load transient response by proposed control method.

DC-link, and the settling times are 340 V and 0.09 s, respectively. The maximum error ratio which is compared to the voltage command of the DC-link voltage is 10.5%. Therefore, the steady-state and transient operation of the proposed topology is confirmed.

4.2 Experimental waveforms of 1-kW prototype

The experimental verifications using a 1 kW prototype has been done. The experimental condition is the same as table 1. The ceramic capacitors are connected in parallel with three capacitors for the buffer capacitor and parallel with two for the filter capacitor, respectively.



Fig. 12. Experimental waveforms at 1 kW.

A gain of the frequency characteristic of the current control is stable in a region of several ten kilohertz in the DCM [17]. Thus, the inductor current is fed by an open-loop control in the experiment.

Figure 12 shows experimental waveforms when the prototype operates at 1 kW. In Fig. 12 (a), when the current reference i_{buf}^* is not applied, the input current oscillates at twice the grid frequency. This current oscillation affects the MPPT efficiency. By contrast, in Fig. 12 (b), the buffer capacitor voltage is oscillated at twice the grid frequency with an oscillation range of 160 V by inserting i_{buf}^* , and the ripple of the input current can be significantly reduced. Therefore, the power ripple is confirmed to be compensated by the proposed control strategy.

4.3 Harmonics analysis of boost inductor and DC-link voltage

1) Boost inductor current

Figure 13 shows a harmonics analysis result of the boost inductor current, which is normalized by its 100-Hz component without the voltage oscillation control as 100%. Note that the number of the harmonic is based on 50 Hz as the fundamental grid frequency. From Fig. 13, the 2nd-order harmonics of the boost inductor current can be reduced by 90.2%. Thus, the power ripple compensation by the proposed power decoupling active power decoupling circuit in DCM is confirmed.

2) DC-link voltage

Figure 14 shows a harmonics analysis result of the DC-link voltage. The results are normalized by the DC components as 100%. The 2nd-order harmonics of the DC-link voltage is less than 1% regardless of the voltage oscillation control of the buffer capacitor voltage. Therefore, the proposed control strategy can control the buffer capacitor voltage without a harmful effect to the DC-link voltage.

4.4 Measured efficiency characteristic respect to output power

Figure 15 shows the measured efficiency characteristic in the 1kW prototype. The switching frequency of the DC-DC conversion is set to 20 kHz. From Fig. 15, the active power decoupling circuit in DCM keeps the efficiency over 94.0% in region of more than 20% of the rated power. In particular, the maximum efficiency reaches 96.0% when the output power is 650 W.



5. Comparison of Efficiency and Power Density of Conventional and Proposed Active Power Decoupling Methods

5.1 Selecting the electrolysis capacitors of passive power decoupling method

In this paper, the electrolytic capacitors of the passive power decoupling method are decided from the allowable ripple current. The current flowing into the electrolytic capacitors includes not only the power ripple component but also the switching frequency component caused by the VSI. The capacitor ripple current is a function of the output power factor and the modulation index, which becomes a nonlinear value [18]. The effective value of the capacitor ripple current is expressed by

$$I_{rms cap} = K_{cap}(\phi, m)I_m$$
 (9)

where ϕ is the output power factor, *m* is the modulation index and $K_{cap}(\phi, m)$ is the coefficient regarding to the ripple current obtained.

Figure 16 shows the $K_{cap}(\phi, m)$ obtained by an electrical circuit simulation. For instance, when the unity power factor in the output and the modulation index of 0.74 from $V_m = 282$ V divided by $V_{dc} = 380$ V, the $K_{cap}(1, 0.74)$ is 0.56 from Fig. 16. Then, the allowable ripple current is calculated by

with the frequency multipliers, where I_{100Hz} is the effective current whose frequencies are twice the grid frequency, I_{nsw} is the effective current at the switching frequency, K_{100Hz} and K_{sw} are the frequency multipliers at 100 Hz and the switching frequency, respectively. Thus, the electrolytic capacitor, which has an allowable ripple current higher than the result of (10), should be required. The volume becomes smaller by parallel connection of capacitors, which has small allowable ripple current when selecting the electrolytic capacitor under the condition of the same rating voltage. In this paper, the electrolytic capacitors which have allowable ripple current of 1 A per one is connected in parallel to satisfy the ripple current requirement with a margin of 50%.

5.2 Design flow for conventional active power decoupling circuits

Figure 17 explains the proposed flowchart for designing the active power decoupling circuit. Firstly, the capacitance is decided from the aspects of the voltage and the storage energy of (3). The capacitance in the active power decoupling circuit is calculated by

In the active power decoupling circuits, the voltage of the buffer capacitor is controlled to large Δv_c . Then, the required storage energy is achieved with small capacitance. This is the principle to be able to reduce the capacitance in the active power decoupling circuits. The capacitor volume is determined from the present products. Note that the average voltage of the buffer capacitor is calculated by using the maximum and minimum of the buffer capacitor voltage as following:

$$v_{ave} = \frac{1}{2} \Delta v_{c} + v_{\min} = \frac{1}{2} (v_{\max} - v_{\min}) + v_{\min}$$

= $\frac{1}{2} [(v_{dc} - \alpha v_{dc}) - (v_{in} + \alpha v_{in})] + (v_{in} + \alpha v_{in})$ (12)



Fig. 16. Current coefficient for calculation of ripple current flowing into DC-link capacitor in DC to single-phase AC converter.



Fig. 17. Design flowchart of active power decoupling circuit.

where v_{max} is the maximum voltage of the buffer capacitor, v_{min} is the minimum voltage of the buffer capacitor and α is the voltage margin of 10%.

Secondly, the switching devices are also selected from the present products. As a margin of withstand voltage, the voltage rating is set to more than 1.5 times of the maximum voltage applied to the semiconductors. For the boost-type active power decoupling circuit, the switches of S_{b1} and S_{b2} are decided by the buffer capacitor voltage. On the other hand, the DC-link voltage limits the voltage rating of the S_{b1} and S_{b2} in the buck-type active power decoupling circuit. For the MOSFETs, a margin of the rated current is set to about 5 times of the effective current in this paper.

Thirdly, the inductance of the inductors is designed based on an allowable current ripple Δi_{buf} in the conventional boost-type active power decoupling circuit. The inductance becomes the maximum value when the voltage difference between the DC-link and the buffer capacitor reaches the maximum. Thus, the inductance is calculated by (13) with current ripple of 30 % in this paper.

$$L_{buf} = \frac{v_{dc}}{\Delta i_L f_{sw}} \frac{\left(v_{ave} + \frac{\Delta v_c}{2}\right) - v_{dc}}{v_{ave} + \frac{\Delta v_c}{2}}$$
(13)

where f_{sw} is the switching frequency in the active power decoupling

d

circuit.

On the other hand, in the conventional buck-type active power decoupling circuit, the inductance of the smooth inductor becomes the maximum value when the capacitor voltage is a half of the DClink voltage. Thus, the inductance is designed by

The inductor volume depends on many parameters of the components. There are several ways to select the core for the inductor. In this paper, the inductor is designed by Area Product concept, which is using the core window area and the cross-sectional area [19]. The inductor volume of the inductor is calculated by

$$Vol_{Lbuf} = K_{v} \left(\frac{L_{buf} I_{max}^{2}}{K_{u} B_{max} J}\right)^{\frac{3}{4}}$$
(15)

where K_v is the volume coefficient depending on the shape of cores, I_{max} is the maximum current flowing to the inductor, K_u is the window utilization factor, B_{max} is the maximum flux density of core, and J is the current density of wire. In this paper, $B_{max}=1.2$ T of a characteristic of nanocrystal line amorphous soft magnetic metal is used. The inductor volume is calculated from $K_v=13.4$, $K_u=0.7$ and J=4 A/mm2 based on a present product of a toroidal coil.

A volume of a cooling system is calculated from a required thermal resistance which is decided by losses caused by the semiconductors. The required thermal resistance $R_{th(f-a)}$ is calculated from

where T_j is the junction temperature of the switching device, T_a is the ambient temperature, P_{loss} is the loss caused by the semiconductors, $R_{th(j-c)}$ is the thermal resistance between the junction and the case and $R_{th(c-f)}$ is the thermal resistance between the case and the cooling system. In order to estimate the volume of the cooling system, CSPI (Cooling System Performance Index) is introduced in this paper [20]. The CSPI means a cooling performance per unit volume of the cooling system. The cooling system is miniaturized when the CSPI becomes higher by the forced cooling system [19]. However, the system lifetime is limited by these fans. Thus, the cooling system is desirable to be designed on the assumption that natural cooling is applied. The volume of the cooling system $V_{olheatsink}$ is provided by [19].

$$VoL_{heatsink} = \frac{1}{R_{th(f-a)}CSPI}$$
 (17)

Finally, in order to clarify the maximum power density point, a Pareto-front of an efficiency η and a power density ρ_{power} is obtained with switching frequency as a variable.

5.3 Design method of the proposed buck-type active power decoupling circuit in DCM

The designing flow shown in Fig. 17 is applied to the proposed active power decoupling circuit in DCM. In the active power decoupling circuit in DCM, the voltage rating of all of the semiconductors is decided from the DC-link voltage. Thus, the switching devices with low rating voltage can be used.

In the equivalent current waveforms of Fig. 7, the duties of each

operation decided from the output power, the voltages and the current peak are obtained by

$$d_{2} = \frac{v_{in}}{v_{dc} - v_{in}} d_{1}$$
(19)

$$u_4 - \frac{1}{v_{buf} - v_{in}} u_3 \qquad (21).$$

In order to avoid the interference between the two operations, the total of the duties is always necessary to meet the condition of (22).

$$d_1 + d_2 + d_3 + d_4 \le 1$$
(22)

The current mode transits from DCM to CCM through the critical current mode (CRM) when (22) exceeded to 1. In the active power decoupling circuit in DCM, the CCM is undesirable current mode because it makes the impossibility of the energy discharge of the inductor to the buffer capacitor or the DC-link capacitor. The current ripple of the inductor is minimized when the proposed active power decoupling circuit operates in the CRM. As a result, the conduction losses caused by the semiconductors and the boost inductor are minimized. Thus, this paper focuses on the CRM condition to design the circuit parameters of the active power decoupling circuit in DCM. The inductance of the boost inductor in CRM is calculated by

where a_{bd} is the boost ratio of the average voltage of the buffer capacitor to the DC-link voltage and a_{di} is the boost ratio of the DC-link voltage to the input voltage. The inductor volume can be estimated from (15).

The volume of the cooling system can be also estimated from (17). The conduction loss of the semiconductors is calculated by (24) from the boost inductor current, and duties $d_1 \sim d_4$.

$$P_{loss_cond} = \frac{I'_{on}}{3T_{out}} \left[\int_0^{T_{out}} i_{peak}^2 (d_1 + d_2) dt + \int_0^{T_{out}} i_{peak}^{2} (d_3 + d_4) dt \right] (24)$$

where T_{out} is the period time of the grid, and r_{on} is the on-resistance of the semiconductors.

Figure 18 describes the patterns when the switching loss happens. The total switching loss is sum of the turn-on loss, the turn-off loss, the recovery loss in the free-wheeling diode (FWD) and the loss caused by the parasitic capacitor discharge. In the active power decoupling circuit in DCM, the turn-on loss does not occur because of zero current switching (ZCS). On the other hand, the turn-off switching loss is caused near the current peak. Therefore, the turnoff switching losses are given by

Topology	Symbol	Component	Rating at 100°C
Passive	C_{dc}	Nippon Chemi-Con EKMZ451VSN181MP30S	450 V, 1.0 Arms 180 μF
Boost chopper	$\mathbf{S}_{c1}, \mathbf{S}_{c2}$	ROHM SiC-MOSFET, SCT3022AL	650 V 65 A
Boost type _ active power decoupling ⁻	C_{buf}	Murata Manufacturing EVS20329S2G306MS09	400 V 30 μF
	C_{f}	Murata Manufacturing KC355WD72E225MH01	450 V 1 μF
	$\mathbf{S}_{b1}, \mathbf{S}_{b2}$	ROHM SiC-MOSFET, SCT3040KL	1200 V 39 A
Buck type	$S_{b1,}S_{b2}$	ROHM SiC-MOSFET, SCT3030AL	650 V 49 A
Proposed circuit	S ₁ -S ₄	ROHM SiC-MOSFET,SCT3017AL	1200 V 83 A

Table 2. Selected components for 3 kW system.

where e_{off} is turn-off energy per the switching, E_{dcd} and I_{md} are the voltage and the current under the measurement condition referred to the datasheet. The recovery loss of S₁ and S₃ does not occur because the FWDs are turned off naturally. However, when S₁ and S₃ turn on, the losses are caused by the discharges of the parasitic capacitors and calculated by

$$P_{sw_{on_{s1}}} = \frac{3}{4} C_{dc} v_{in}^{2} f_{sw}$$
(27)
$$P_{sw_{on_{s2}}} = \frac{1}{4} C_{ds} \left(v_{buf} - v_{in} \right)^{2} f_{sw}$$
(28)

where C_{ds} is the capacitance between the drain and the source of the switching device. From (25)-(28), the switching loss proportionally increases with the increase of the switching frequency.

5.4 Theoretical evaluation of proposed active power decoupling circuit in DCM in terms of efficiency and power density

Table 2 shows the selected components assumed to be used in 3kW system of each circuit topology. The inverter output power of 3-kW, the input voltage of 150 V, the DC-link voltage of 380 V, the inverter output voltage of 200 V with 50 Hz are assumed. Fig. 18 shows the Pareto-front of the efficiency and the power density with the switching frequency as a variable in the DC-DC converter with the power decoupling circuits. In Fig. 18, the losses caused by the semiconductor and the resistive loss of the capacitor are considered.

In the active power decoupling circuits, the ceramic capacitor with high energy density is selected as the buffer capacitor. The parallel number of the ceramic capacitors is decided from (11) with consideration of capacitance reduction effect due to the DC bias. The current ripple of the inductor is set to 30% of the peak current. The switching frequency in the active power decoupling circuits is assumed to be same as in the boost chopper. The boost inductor in the active power decoupling circuit in DCM is designed based on the CRM condition. In Fig. 18, the power density of all of the circuit topologies increases with the increase of the switching frequency at the beginning, because the inductor volume can be reduced. However, the heatsink volume increases due to the deterioration of the switching loss. As a result, with increasing the switching frequency, the power density decreases after reached at the



Fig. 18. Calculated Pareto-front of DC-DC conversion with passive or active power decoupling circuits.



Fig. 19. Component volume distribution at the maximum power density points.



Fig. 20. Loss distribution at the maximum power density points.

maximum value.

According to Fig. 18, the maximum power density of the passive power decoupling method is 9.3 kW/dm³ with the efficiency of 98.8% when the switching frequency is 35 kHz. The conventional active power decoupling circuits in the boost-type and the bucktype reaches 9.5 kW/dm³ at 45 kHz and 9.9 kW/dm³ at 45 kHz respectively. By contrast, the active power decoupling circuit in DCM approaches 10.8 kW/dm³ with efficiency of 98.8% when the switching frequency is 20 kHz. Therefore, the maximum power density in the proposed active power decoupling circuit in DCM is 115% and 108% compared with in the passive and the conventional buck-type active power decoupling circuit, respectively.

Figure 19 shows the volume distributions of the components at the maximum power density point of each circuit topology. The component volume is normalized with the volume of the passive power decoupling method as 100%. The active power decoupling circuit in DCM reduces the inductor volume by 30.4% when compared to the conventional buck-type active power decoupling circuit. As a result, the total volume is reduced by 7.2%.

Figure 20 shows the loss distributions at the maximum power density point of each circuit. These results are normalized with the total loss of the passive power decoupling method as 100%. The total loss of the active power decoupling circuit in DCM is 98.7% of that of the passive power decoupling method. The conduction loss of the chopper caused by S_1 and S_2 accounts for 45.9% of the whole in the active power decoupling circuit in DCM. This is because the effective current flowing to the switching devices is increased due to the higher current peak of the DCM.

6. Conclusion

This study proposed a novel buck-type active power decoupling circuit operated in DCM to be applied to a DC to a single-phase AC converter. The proposed active power decoupling circuit in DCM absorbs the power ripple by ceramic or film capacitors instead of electrolytic capacitors, a long lifetime can be expected. Moreover, utilizing the current zero cross in DCM for the power ripple compensation, the proposed active power decoupling circuit in DCM doesn't need additional inductors.

The experimental verifications by a 1-kW prototype of the active power decoupling circuit in DCM showed the following results.

(1) A current ripple with twice the grid frequency was reduced by 90.2% by the proposed active power decoupling circuit in DCM.

(2) A voltage ripple of the DC-link is less than 1% against the DC component. A non-interference between voltage controls of DC-link and buffer capacitor can be achieved by utilizing the zero-current period in the DCM.

(3) A conversion efficiency exceeds 94 .0% in the region of 20% of the rated power to 1 kW, especially 96.0% of the maximum at 650 W.

According to a theoretical evaluation in an assumption of a 3-kW system, the following results were clarified through a Pareto-front of power density and efficiency clarified the following results.

(4) The maximum power density of the active power decoupling circuit in DCM is achieved at 20 kHz, and 115 % higher than the electrolytic capacitors of the passive power decoupling method.

(5) Compared to in a conventional buck-type active power decoupling circuit, the proposed active power decoupling circuit in DCM reduces the total inductor volume by 30.4%.

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